CHAPTER-1

→ Semiconductor :- The atom in which normally have four electrons and four holes in the outermost shell is called semiconductor.

• Intrinsic Semiconductor :-

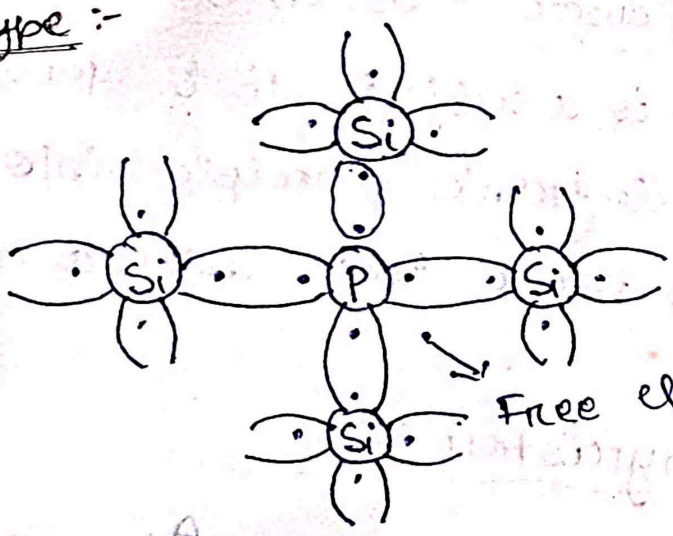
Pure semiconductor which is free from every impurity are called intrinsic semiconductors.

→ Doping :- The process of adding impurities to the intrinsic semiconductor is called doping.

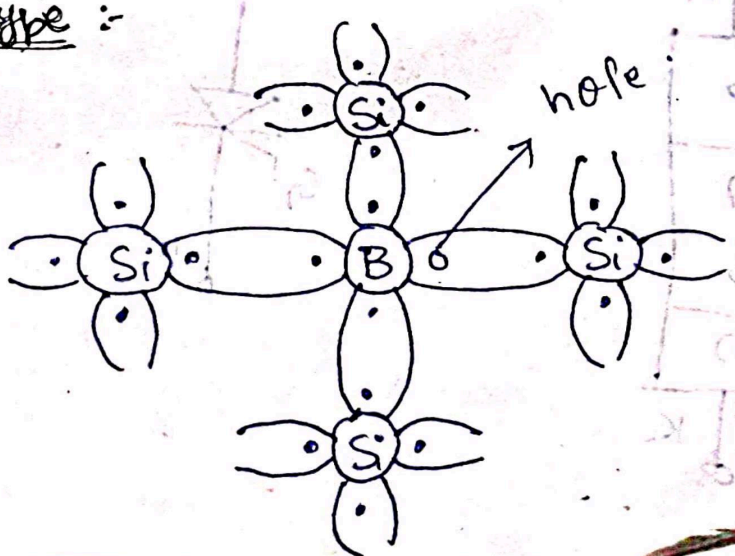
→ Extrinsic Semiconductor :-

After doping, the semiconductor is known as extrinsic semiconductor

→ N-type :-



→ P-type :-



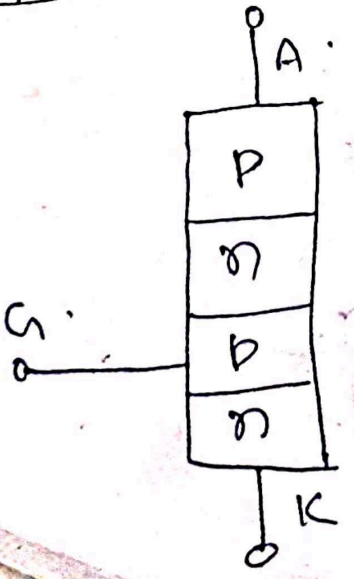
* Avalanching Effect

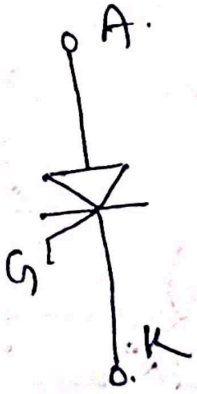
The avalanching effect occur when the potential difference between the p-n junction becomes so high that free electrons crossing the junction gain enough energy to knock the covalent bond and breaks that bond and the electrons becomes free. This collision create a new hole-electron pair. The process then repeat causing a chain of reaction almost instantly a huge amount of charge carriers are generated and it breaks the p-n junction.

* Introduction to Power Electronics :-

Power electronics is a subject that deals with the application of electronic principle into a situation that are rated on power level instead of signal level.

* Principle of Thyristor :-

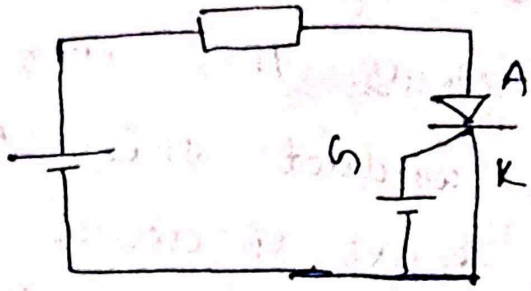




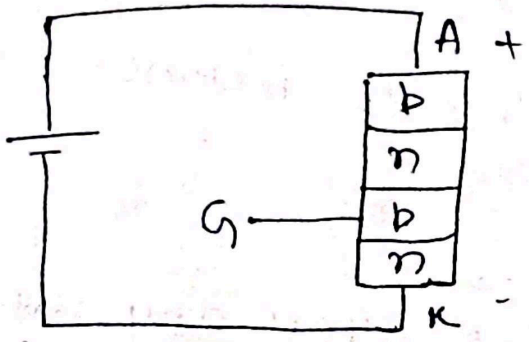
→ Reverse Blocking mode

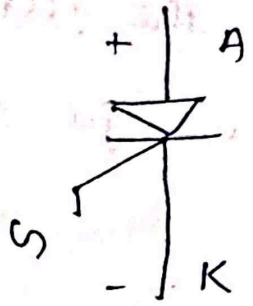
→ Forward Blocking mode

→ Forward conduction mode



* Principle & operation of Thyristor :-





→ It is a p-n-p-n switching device having 3-junctions J_1, J_2 & J_3.

→ It has 3-external terminals i.e., Anode, cathode & gate.

→ The anode & cathode are connected to main power supply & the gate is connected to inner p-layer.

→ When the end p-layer is made +ve w.r.t end n-layer. Then, the outer junction J_1 & J_3

→ Then, the outer junction J_1 & J_3 are foowar biased and the inner junction J_2

is reverse biased. Thus junction J_2 has a depletion layer which doesn't allow any current to flow through the device only a small amount of leakage current flows. This current is insufficient to make the device conduct this state is called forward blocking mode of device.

→ When the end n-layer made positive w.r.t end p-layer, the junction J_2 becomes forward biased and junction J_1 & J_3 becomes reverse biased.

→ Junction J_1 & J_3 doesn't allow any current to flow through the device only a small leakage current flows & the state is known as reverse blocking mode.

→ If the voltage increases depletion layer J_2 vanishes due to avalanche breakdown. Since junction J_1 & J_3 are already forward biased there will be a free carrier movement across the 3-junctions. Then, this state is called forward conduction mode.

* State V-I characteristics of SCR.

→ Reverse Blocking mode :-

When cathode is made positive w.r.t anode with switch 'S' (gate switch) open, SCR is reverse biased.

→ Junction J_1 & J_3 are reverse biased and junction J_2 is forward biased. A small leakage flows in reverse blocking mode. It is shown in the graph.

→ If reverse voltage is increased to a critical breakdown level called reverse voltage breakdown and avalanche breakdown occur and the junction J_1 & J_3 breaks and current flows in high rate.

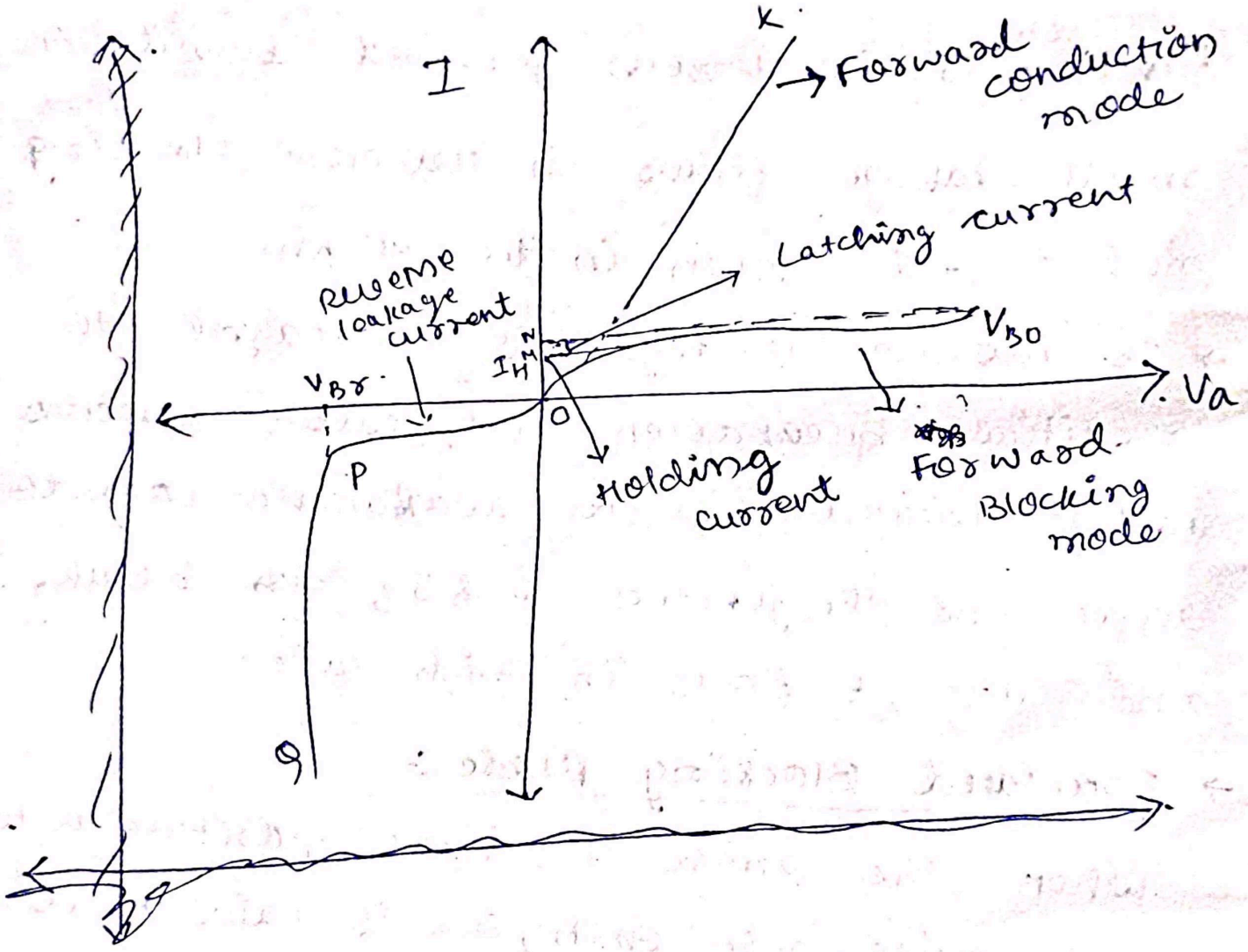
→ Forward Blocking mode :-

When the anode is made positive w.r.t cathode with gate open, SCR is said to be forward biased junction. J_1 & J_3 are forward biased and junction J_2 is reverse biased

→ In this mode, a small leakage current flows as shown in fig.

It represents the forward blocking mode of SCR.

As the forward leakage current is so small SCR offers a high ~~re~~ impedance so, it can be treated as a switch.



* **Forward conduction mode**

When the anode is made positive w.r.t cathode then junction J_1 & J_3 is forward biased and junction J_2 is reverse biased. If we increase the voltage then the junction J_2 will have an avalanche breakdown at a voltage is called forward breakover voltage (V_{BO}). After this breakdown, the thyristor get turn on with point 'M' and shifted to 'N' then anywhere between N & K. Here N, K represented as forward conduction mode.

* **Latching Current (I_L):-**

It is the minimum amount of anode current above which the thyristor will hold the conduction state irrespective of the gate current.

* **Holding Current (I_H) :-**

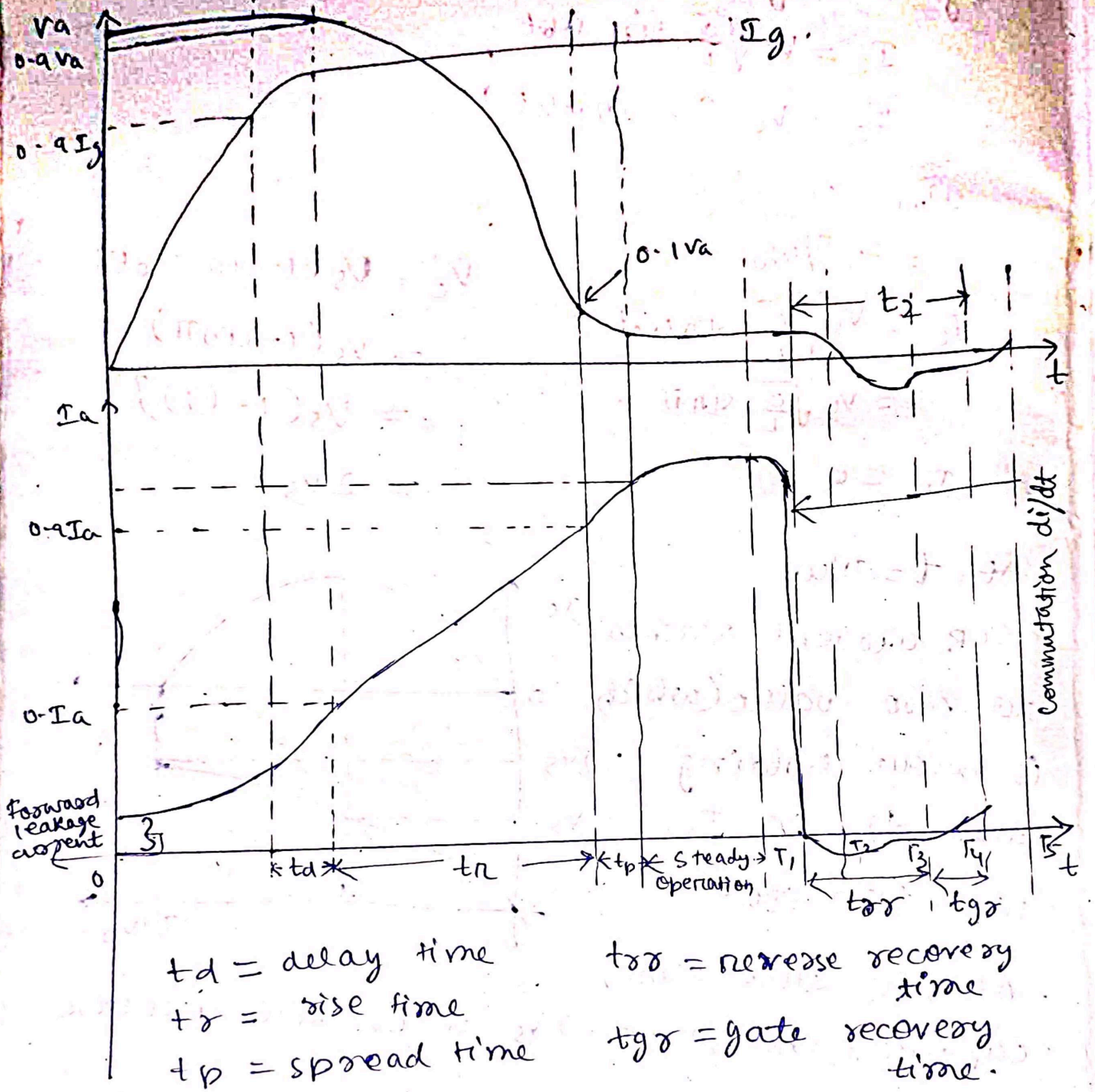
It is the minimum anode current below which thyristor will jump from conduction state to blocking state.

$\Rightarrow V_s - V_t + 2V_s = 0$

$\Rightarrow \boxed{V_t = -V_s}$

The conduction period of SCR depend upon the commutating component L & C.

Dynamic Mechanism of SCR



t_d = delay time

t_r = rise time

t_p = spread time

t_{rr} = reverse recovery time

t_{gr} = gate recovery time.

* Dynamic Mechanism of SCR

The time variation of voltage across SCR & current through it during TURN ON &

turn OFF process gives the dynamics (transient behaviour of thyristor).

The total turn ON time is divided into 3 parts:

(1) Delay Time (t_d)

(2) Rise Time (t_r)

(3) Spread Time (t_p)

(1) Delay Time (t_d)

It is the time ~~delti~~ duration between 90% of gate current to 90% of anode current. By the application of gate signal to the p-layer, the current is non-uniformly distributed. Its (gate current) value is highest near the gate.

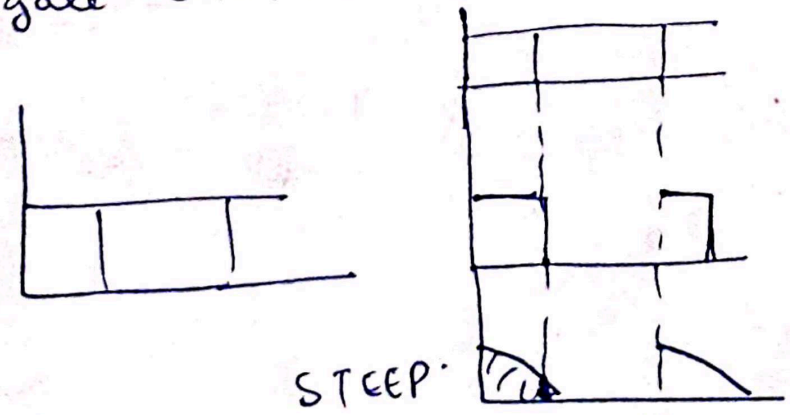
→ During delay period, current flows in a narrow region near the gate where the current density is highest.

The delay time can be decreased by increasing more amount of gate current & more amount of anode to cathode voltage.

(2) Rise Time (t_r):-

The time duration between 10% of anode current to 90% of anode current. The rise time is inversely proportional to the magnitude of gate current & its built-up rate.

The rise time can be decreased by applying steep gate current pulses.



Steep → sudden rise of current

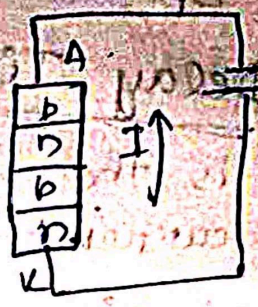
(3) Spread Time :-

It is the time taken by the anode current to rise 90% of anode current to 100% anode current. During this period the conduction spreads over entire cross-section of P-layer.

The spreading time depends upon the gate structure of SCR. After spread time it attends a steady value & voltage drop across SCR which is equal to 1 to 1.5 V

* Turn-OFF Mechanism :-

Turn off time of a thyristor is defined as the time between the instant of anode current becomes zero & the instant it regains the forward blocking capability.



During Turn OFF period, all the excess charge carriers from the 4-layer must be removed. The carrier around the junction J_2 can be removed by the process of recombination.

The total turn OFF time can be divided into two parts -

(i) Reverse recovery time (t_{rr})

(ii) Gate recovery time (t_{gr})

At time 't_1' anode current is zero. After 't_1' there is some stored charge present in 4-layer. The reverse recovery current removes the excess charge carrier.

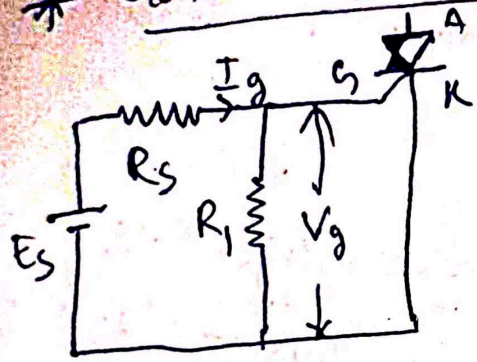
Due to reverse recovery period, we sweep out holes from p-layer & electrons from n-layer. At the end of reverse recovery period, the junction 'J_2' has trapped certain charges.

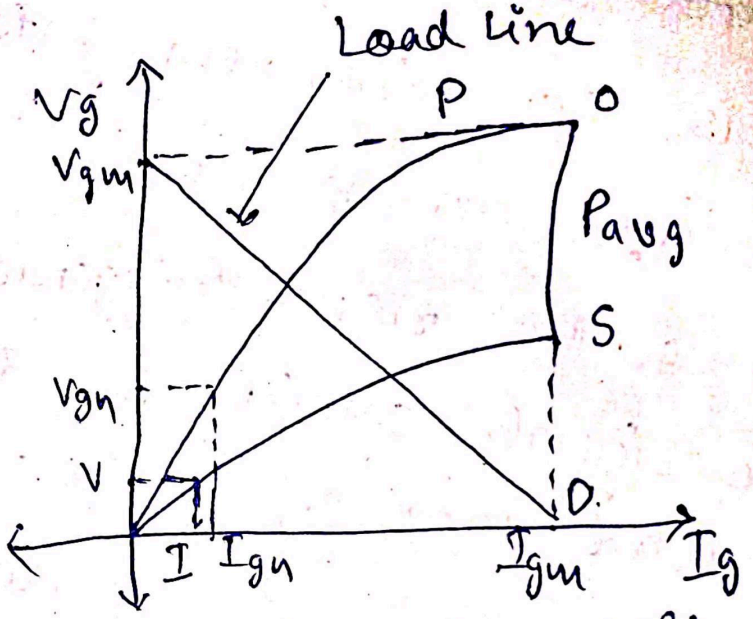
These trapping charge can be removed by the process of recombination. From T_3 to T_4 the charge can be removed by the process of recombination which is present near the gate. This time is known as 'gate recovery time'.

The turn OFF time can be decreased by increasing the reverse voltage.

The circuit turn-OFF time is defined as the time between the instant anode current becomes zero & the instant reverse voltage due to practical circuit reaches zero. Time T_c must be greater than T_2 for reliable turn OFF otherwise the device may turn ON at an undesired instants. The process is called

* Gate characteristics :-





It is the characteristic between voltage across gate cathode (V_g) and current through the gate.

→ The curve OS is the lowest voltage value that can be applied to turn on the SCR.

→ The curve OP is the highest permissible voltage that can be applied for safe operation of the gate circuit.

→ V_{gm} is the maximum gate voltage that can be applied for the safe operation.

→ I_{gm} is the maximum gate current that can be applied for the safe operation.

→ P_{avg} is the average power dissipation that can be permissible for the reliable operation of the SCR.

→ OX is the minimum gate current required to turn on the SCR.

→ OY is the minimum gate voltage required to turn on the SCR.

→ Oa is the non-triggering voltage, the noise signal should be below this to avoid unwanted turn on of the SCR.

→ To know the gate operating point, we have to draw the load line which is the line between maximum possible gate voltage and

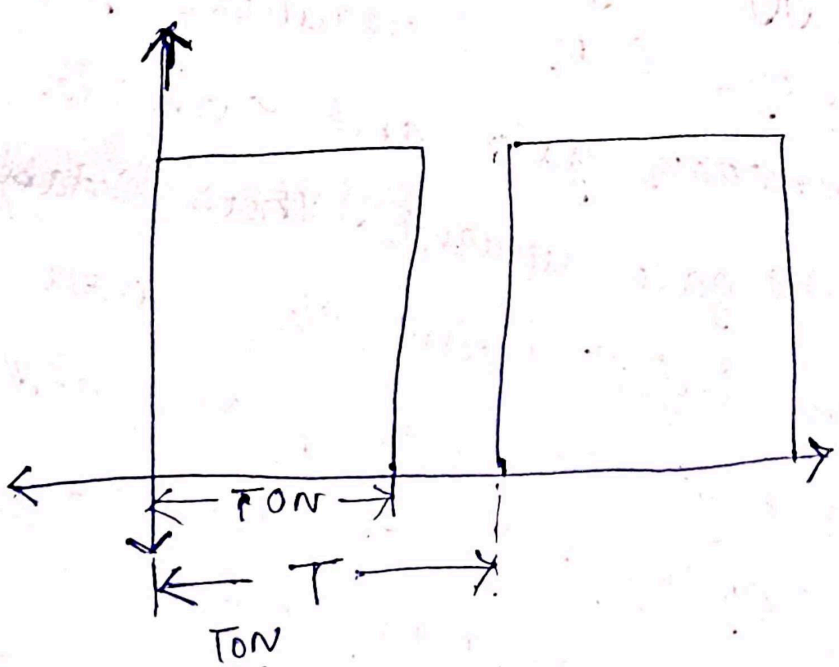
maximum possible gate current.

→ The gradient of load line ($HD = \frac{OH}{OD}$) will give the required gate source resistance (R_s).

→ R_1 is the resistance that bypass the leakage current if exists there in.

→ Always, we prefere pulse type gate signal rather than continuous gate signal to reduce unnecessary gate loss.

* **Duty Cycle** :- A duty cycle is defined as the ratio of pulse on period to the period in given time of pulse.



$$\partial = \frac{T_{ON}}{T}$$

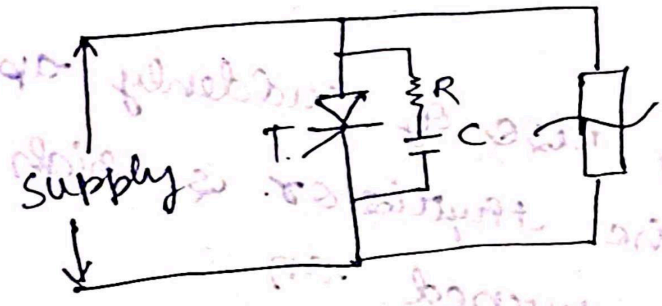
$$P_{avg} = \frac{1}{T}\int_0^{T_{ON}} P_{gm}\, dt$$

$$= \frac{1}{T} P_{gm} \left[T\right]_0^{T_{ON}}$$

$$= \frac{1}{T} P_{gm} \left[T_{ON} - 0\right].$$

When switch S is closed, a sudden voltage appears across the circuit. Capacitor 'C' behave like a short-circuit and the current bypass through the capacitor. Then, the capacitor charges to the voltage V_c. When the SCR is turned on, capacitor discharges through the SCR & send a current equals to "$\frac{V_s}{R_s}$".

- External Over-voltage



External over-voltage are caused by -

(i) Interruption of current flow in the inductive circuit.

(ii) Due to lightning stroke

(iii) when the thyristor is connected through a T/F, transient is to occur due to magnetising & demagnetising of T/F core.

Suppression of over voltage :-

The effect of over-voltage can be minimised by a non-linear resistor connected across the SCR.
(It has a falling resistance characteristic with increase of voltage)
The examples are Selenium, Thyrector diode, Metal oxide varistors, Avalanching diode.

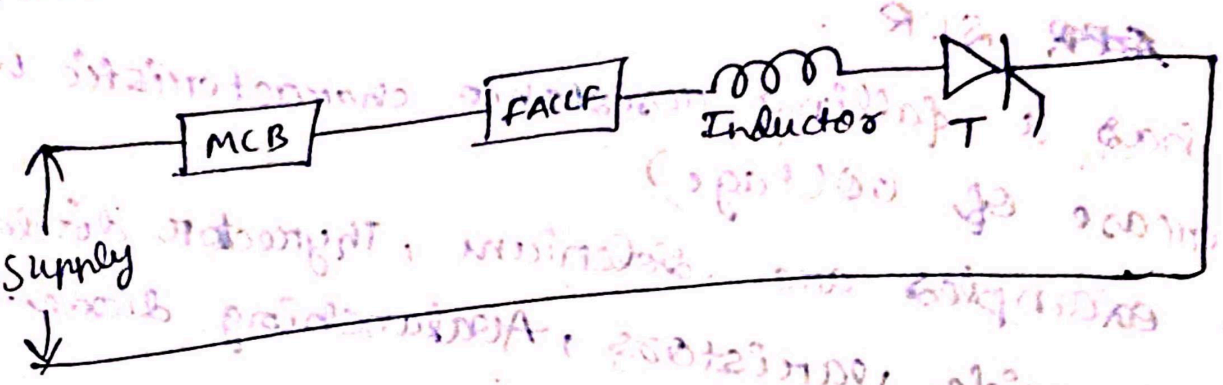
⇒ Over-Current protection

over-current occurs due to fault, short circuit or due to surge current, so, the junction temperature increases & the device may get damaged.
Circuit Breaker & fast Acting Current Limiting Fuse are used for over-current protection.

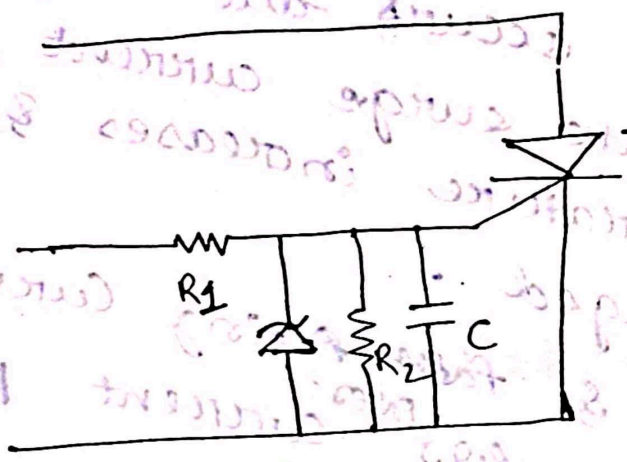
$\frac{di}{dt}$ protection :-

When the thyristor is forward biased & is turned on by a gate pulse, the conduction of anode current begins near the gate-cathode junction. If the rate of rise of anode current is large as compared to the spreading velocity of carriers, a hotspot will be created due to high current density.

So, an inductor is connected in series with the thyristor to oppose the sudden change in current.



* Gate Protection :-



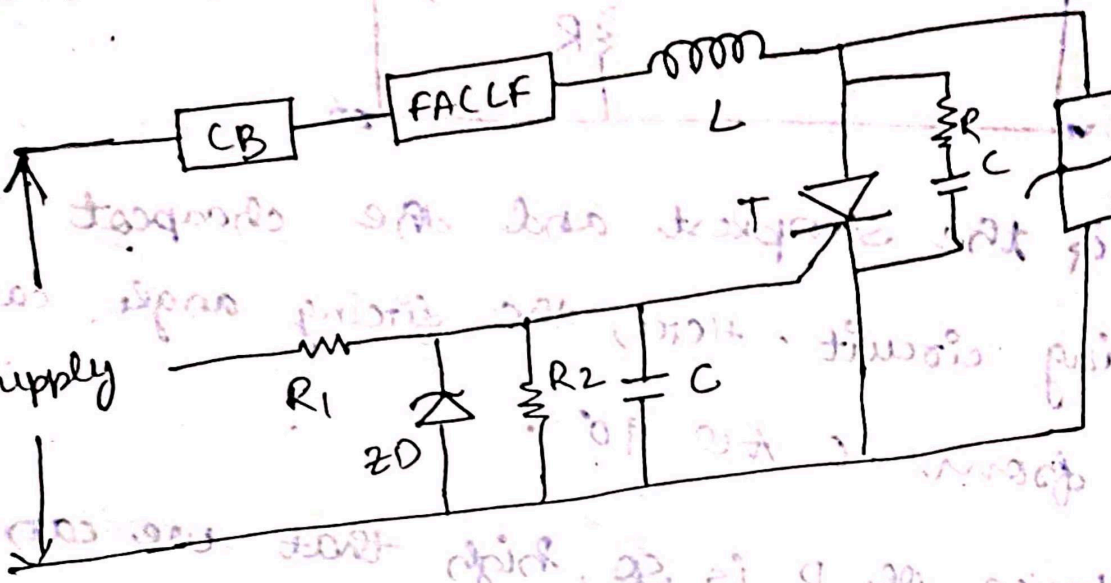
Gate circuit should also be protected against over-voltage & over-current.

Over-voltage across the gate circuit can cause false-triggering of the SCR.

Over current may raise the junction temperature & leads to SCR damage.

Protection against over voltage is achieved by connecting a Zener diode

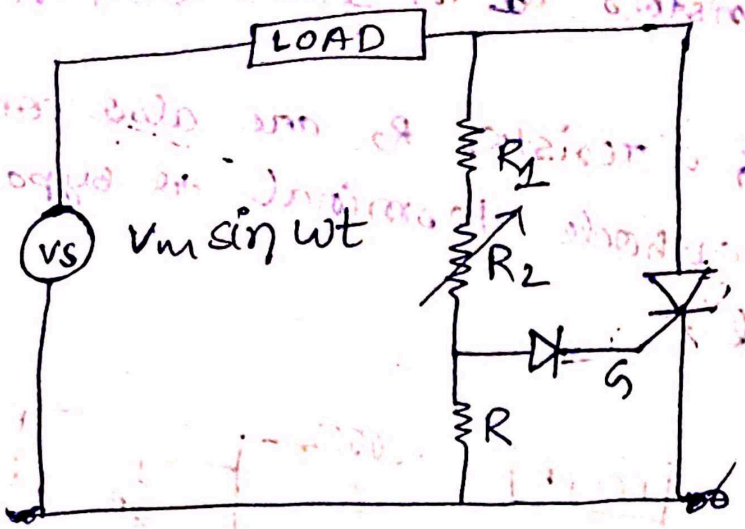
across the gate circuit.
protection against over-current is achieved by connecting a resistor R_1 in series with the gate circuit.
A capacitor & a resistor R_2 are also connected across gate cathode terminal to bypass the noise signal.



* **Triggering** :-
The process of turning ON the thyristors is called triggering that means the process by which the thyristor will jump from forward blocking state to forward conduction state with desired gate signal.

→ **Types of Triggering** :-
(1) Resistance triggering / firing.
(2) R-C triggering.

(1) Resistance Firing / Triggering :-



It is the simplest and the cheapest triggering circuit. Here, the firing angle can be varied from 0 to 90°.

The resistance of R is so, high that we can neglect the load resistance, R_L.

- **Value of R**

Since, the thyristore is in blocking state, the current will flow through the path $V_s - L - R_1 - R_2 - R - V_s$. The resistore R provide sufficient gate - cathoge voltage, so, this resistance is known as stabilising resistance.

The maximum voltage across the resistance R

$$V_R = \frac{V_m R}{R_1 + R_2 + R} \quad [R_2 \neq 0]$$

A simple R-C triggering ckt giving full wave output voltage as shown in the fig:

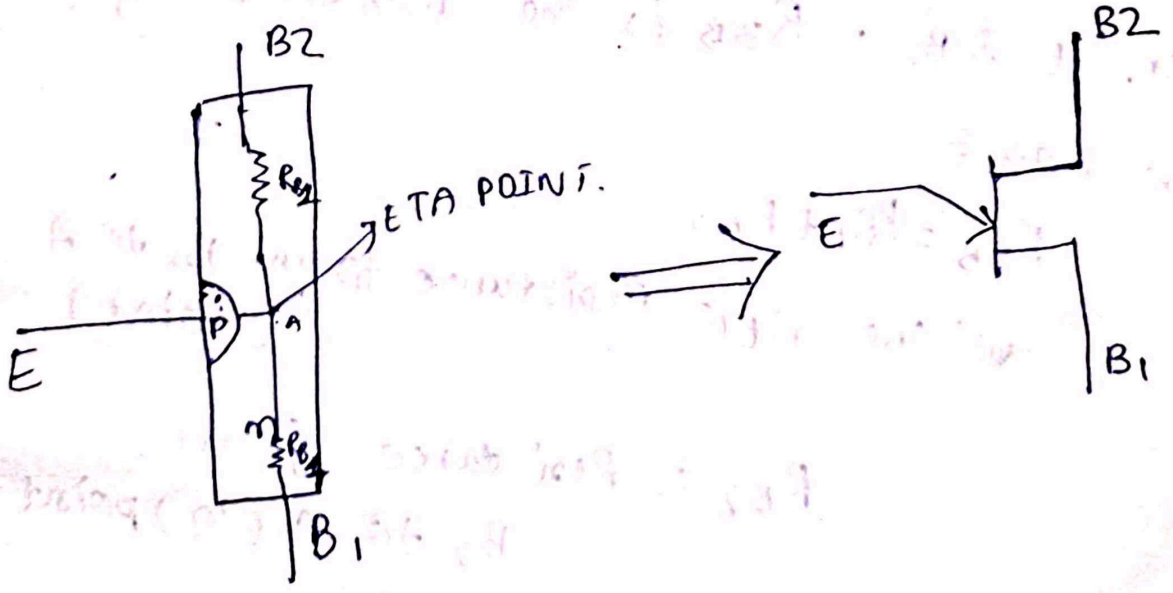
Diode D_1 & D_4 form a full wave bridge rectifier.

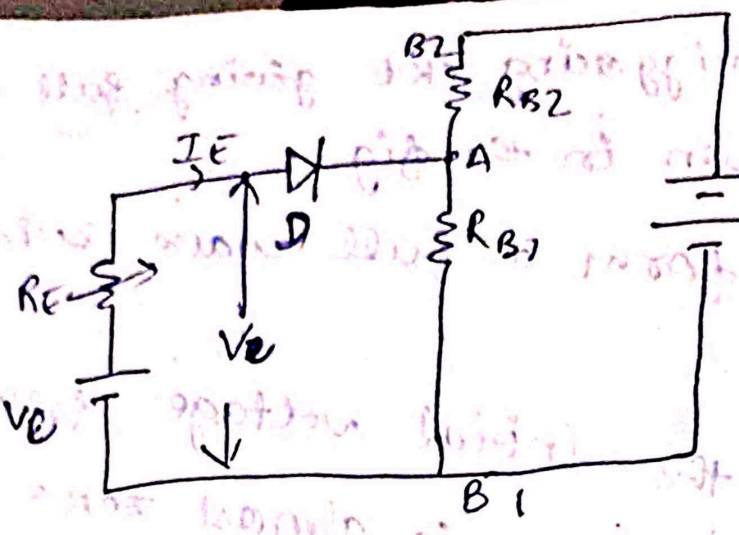
In this circuit, the initial voltage from which capacitor C charges is almost zero. The capacitor C is set to low positive voltage by the clamping action of SCR gate when capacitor charges to a voltage "Vgt" SCR triggers. This will happen in every half cycle.

$$RC \geq \frac{50T}{2} \qquad \left[T = \frac{1}{f}, \; f = \text{supply frequency} \right]$$

$$R \geq \frac{V_s - V_c}{I_{gt}}$$

* UJT (Uni-Junction Transistor) :-





$$V_A = IR = \frac{V_{BB}}{R_{B1}+R_{B2}} \times R_{B1} = \frac{R_{B1}}{R_{B1}+R_{B2}} \times V_{BB}$$

$$\Rightarrow \boxed{V_A = \eta V_{BB}} \quad \boxed{\because \eta = \frac{R_{B1}}{R_{B1}+R_{B2}}}$$

UJT consist of lightly doped n-type base and heavily doped p-type emitter. The two ohmic-contact provided at each end of the base are called base-1 (B_1) & base 2 (B_2).

An emitter base resistance (R_{BB}) exist between B_1 & B_2. R_{BB} is the resistance of n-type bar.

$$R_{BB} = R_{B1} + R_{B2}$$

where, R_{B1} = resistance from B_1 to A (n point)

R_{B2} = Resistance from B_2 to A (n) point.

* Symbolic representation & Equivalent Circuit :-

In the OFF state if we neglect the diode for a movement when voltage V_{BB} is applied.

$$V_A = \left(\frac{V_{BB}}{R_{B1}+R_{B2}}\right) \times R_{B1}$$

$$V_A = \eta V_{BB}$$

where, $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}$.

As long as emitter voltage V_e is less than ηV_{BB}. $E-B_1$ junction (p-n junction) is reverse biased.

Emitter current I_e is -ve as ~~seen~~ shown in the coil P-S.

The region P-S is treated as OFF state of UJT. At point S, $I_e = 0$ & $V_e = V_{EE}$.

By varying 'RE', 'Ve' increases $V_e = V_D + \eta V_{BB}$ at point B is reached.

E-B_1 junction is forward biased at point B is called peak point. At this point voltage is V_p & current is I_p.

At this point $V_p = V_e = V_D + \eta V_{BB}$.

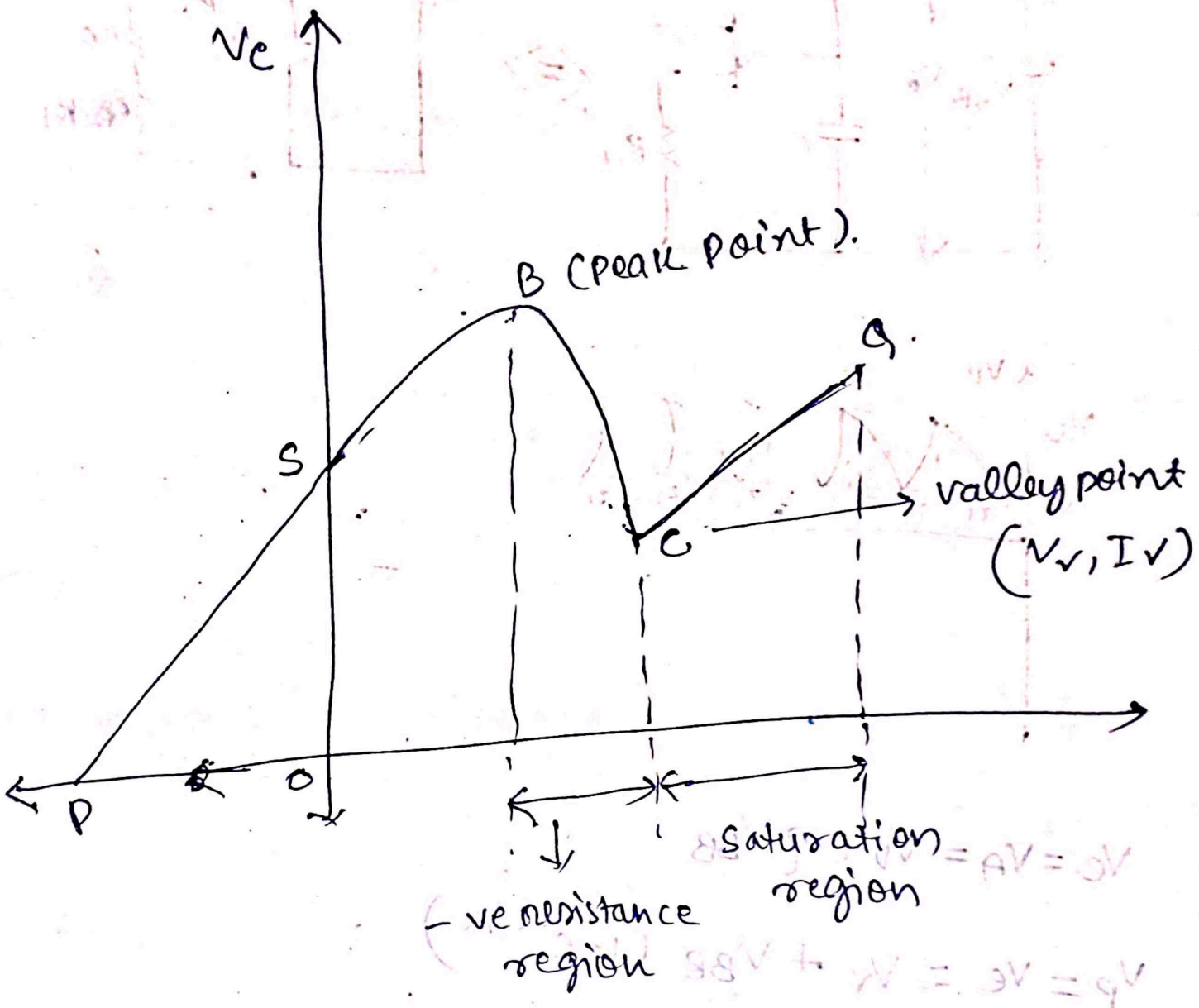
Point B-C is called -ve resistance region.

→ P-emitter begins to inject holes from heavily doped emitter-e into lower base region B_1. As n-type base is lightly doped the holes rarely get chance to recombine. Current carriers (hole) increase in B-region therefore resistance R_{B_1} decreases so, V_A decreases then 'Ve' decreases.

$$I_e = \frac{V_{BB} - V_e}{R_E}$$

I_e increases at point C when resistance decreases to a very small value & reach to point C is the valley point with voltage V_v & current I_v respectively.

After UJT is ON, if Ve increases with Ie increases this indicated by curve Cq.



These driver ICs are designed for general and specific applications

Current type: IR 2110, IR 2111, IR 2112

Special type:

- For square-wave and high voltage: IR 2111
- For resonant and phase shifted PWM: IR 2112, IR 2113
- For buck-boost converters: IR 2125
- For 3-phase, six step, PWM: IR 30, IR 2132
- For oscillating application converters: IR 2155.

5.13 Comparison of IGBT and MOSFET

	IGBTs
MOSFET, the decrease in the electron mobility with increasing temperature results in a rapid increase in the on-state resistance of the channel and hence the on-state drop.	1. In IGBTs, this increase in voltage drop is very small.
2. The on-state voltage drop increases by a factor of 3 between room temperature and 200°C.	2. Here with the identical conditions, the increment in the on-state voltage drop is very small.
3. All highest temperature, maximum current rating goes down to 1/3 value.	3. At high ambient temperature; IGBT is extraordinarily well suited.
4. Current sharing in multiple paralleled MOSFETs is comparatively poor than IGBTs.	4. Current sharing in multiple paralleled IGBTs is far better than power MOSFET.
5. The turn-on transients are identical to IGBTs.	5. Turn-on transients are identical to MOSFETs.
6. Power MOSFET is suited for applications that require low blocking voltages and high operating frequencies.	6. IGBT is the preferred device for applications that require high blocking voltages and lower operating frequencies.

5.16 GATE TURN-OFF THYRISTORS (GTOs OR LATCHING TRANSISTORS)

Previous chapters describes the thyristor and their use in power electronic applications. Also, we have seen that thyristors can block high voltage (several thousand volts) in the off-state and conduct large currents (several thousand amperes) in the on-state with only a small on-state voltage drop (a few volts). The most useful of all is their capability of being switched ON when desired by

means of a control signal applied at the gate of the thyristors. However, as we know that once an SCR is turned ON by the gate signal, the gate loses control and it can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current. This is the serious deficiency in thyristors that prevent their use in switch mode applications. This section describes the structure and operation of thyristors that have a gate turn-off capability, the so-called gate turn-off thyristors or GTOs.

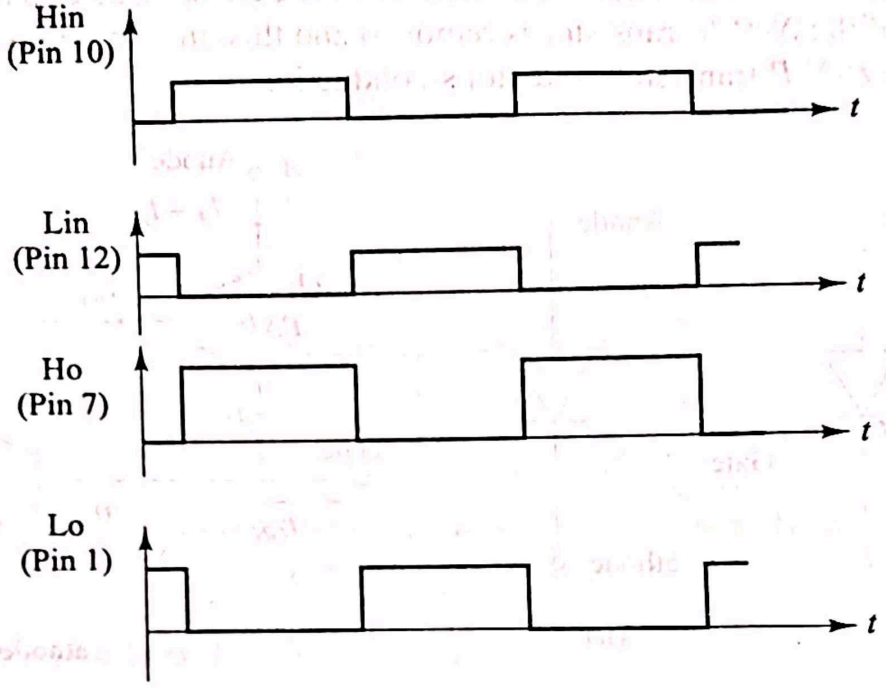


Fig. 5.68 *Typical waveforms for IC 2110*

5.16.1 Basic Structure

The gate turn-off thyristor (GTO) incorporates many of the advantages of the conventional thyristor and the high-voltage switching transistor. It is a *PNPN* device that can be triggered into conduction by a small positive gate-current pulse, but also has the capability of being turned-off by a negative gate-current pulse. However, the turn-off current gain is low (typically 4 or 5). For example, a 4000 V, 3000 A device may need –750 A gate current to turn it OFF. This facility allows the construction of inverter circuits without the bulky and expensive forced commutating components associated with conventional thyristor circuitry. The GTO also has a faster switching speed than the regular thyristor, and it can withstand higher voltage and current than the power transistor or MOSFET.

The GTO is a three-terminal device with anode, cathode and gate terminals. The various circuit symbols are shown in Fig. 5.69. The two-way arrow convention (Fig. 5.69(i)) on the gate lead distinguishes the GTO from the conventional thyristor. Figure 5.70 shows the two-transistor analogy of the GTO. Like the conventional thyristor, the GTO switches regeneratively into the on-state when a positive gating signal is applied to the base of the *N-P-N* transistor. In a regular thyristor, the current gains of the *N-P-N* and *P-N-P* transistors are

large in order to maximize gate sensitivity at turn-on and to minimize on-state voltage drop. But this pronounced regenerative. latching effect means that the thyristor cannot be turned-off at the gate. Internal regeneration is reduced in the GTO by a reduction in the current gain of the *P-N-P* transistor, and turn-off is achieved by drawing sufficient current from the gate. The turn-off action may be explained as follows. When a negative bias is applied at the gate, excess carriers are drawn from the base region of the *N-P-N* transistor, and the collector current of the *P-N-P* transistor is diverted into the external gate circuit. Thus, the base drive of the *N-P-N* transistor is removed and this, in turn, removes the base drive of the *P-N-P* transistor, and stops conduction.

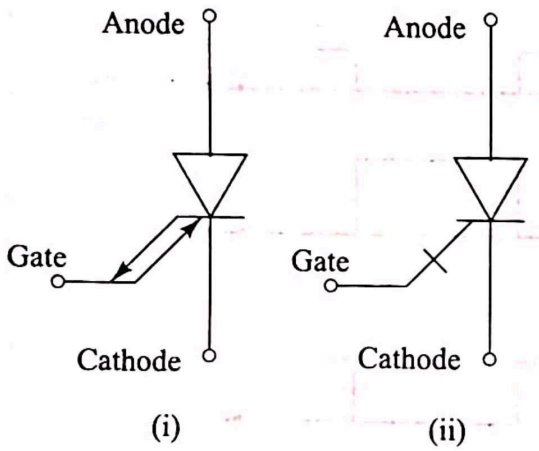


Fig. 5.69 *Circuit symbols*

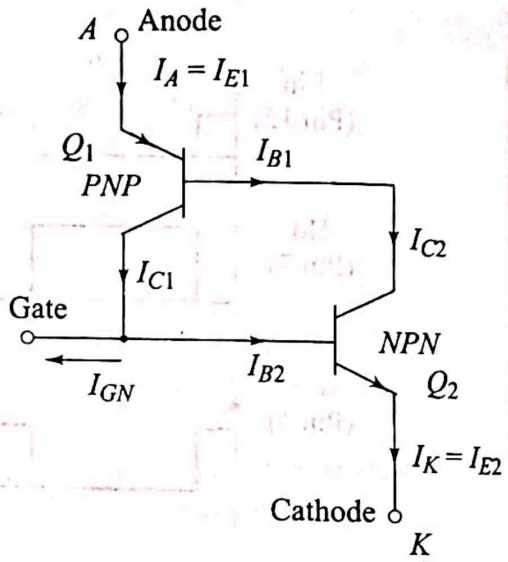


Fig. 5.70 *Two-transistor analogy of GTO*

The reduction in gain of the *P-N-P* transistor can be achieved by the diffusion of gold or other heavy metal to reduce carrier lifetime, or by the introduction of anode to *N*-base short-circuiting spots, as in Fig. 5.71, or by a combination of these two techniques. Device characteristics are influenced by the particular technique used. Thus, the gold-doped GTO retains its reverse-blocking capability but has a high on-state voltage drop. The shorted anode emitter construction has a lower on-state voltage, but the ability to block reverse voltage is sacrificed. Large GTOs also have an interdigitated gate-cathode structure in which the cathode emitter consists of many parallel connected *N*-type fingers diffused into the *P*-type gate region, as in Fig. 5.71. This configuration ensures a simultaneous turn-on or turn-off of the whole active area of the chip.

GTOs are available with symmetric or asymmetric voltage blocking capabilities. A symmetric blocking device cannot have anode shorting and, therefore, is somewhat slower. The use of asymmetrical GTOs requires the connection of a diode in series with each GTO to gain the reverse blocking capability, whereas symmetrical GTOs have the ability to block a reverse voltage. In symmetrical GTOs, *N*-base is doped with a heavy metal to reduce the turn-off time. The

asymmetrical GTOs offer more stable temperature characteristics and lower on-state voltage compared to symmetrical GTOs.

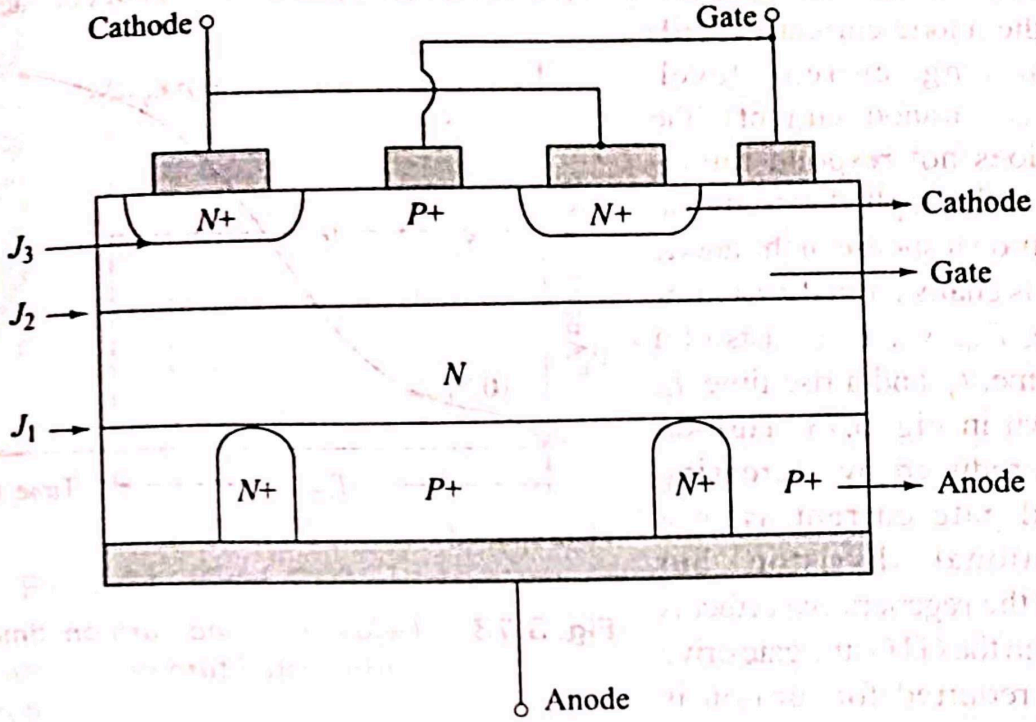


Fig. 5.71 *Basic GTO structure showing anode to N-base short-circuiting spots*

5.16.2 Switching Performance

The simplified gate drive circuit of Fig. 5.72 shows separate d.c. supplies for turn-on and turn-off. The GTO is gated into conduction by means of transistor T_1 in the turn-on circuit. The switching device in the turn-off circuit should have a high peak current capability. An auxiliary thyristor or MOSFET is appropriate for this duty. Figure 5.72 shows an auxiliary SCR, TH_1, which is gated to initiate the turn-off process. Turn-off performance may be enhanced by the presence of some series inductance, L, as shown. The voltage supply for the turn-off circuit is in the region of 10 to 20 V and the gate current at turn-off, applied for few microseconds, is typically about one-fifth of the anode current prior to turn-off . Consequently, the energy required to turn-off the GTO is much less than that needed to turn-off a conventional thyristor.

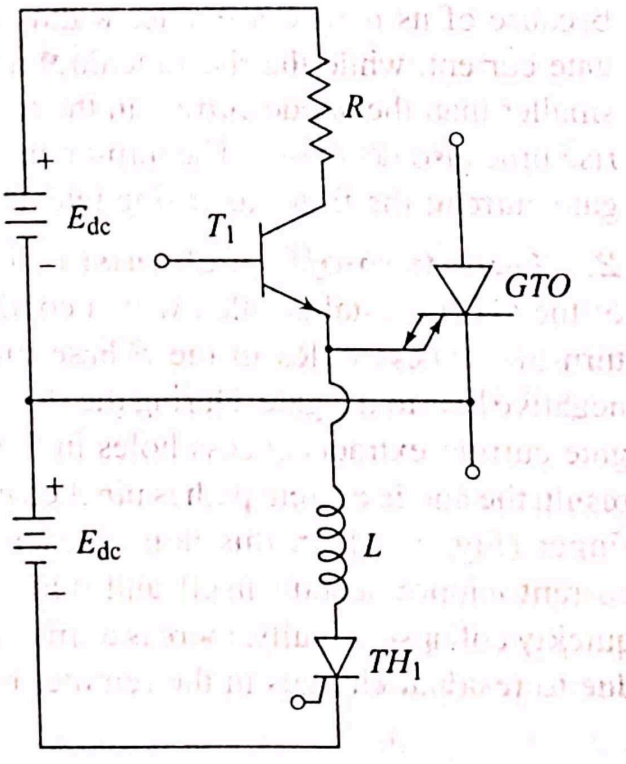


Fig. 5.72 *Basic gate-drive circuit for a GTO*

1. *Gate turn-on mechanism* The gate turn-on mechanism of the GTO is similar to that of a conventional thyristor. A steep-fronted pulse of gate current turns-on the device, and gate drive can be removed without the loss of conduction when the anode current exceeds the latching current level. However, the anode current of the GTO does not respond immediately to the applied gate signal. The turn-on response of the anode current is characterized by a turn-on time, T_{on}, which consists of a delay time, t_d, and a rise time, t_r, as shown in Fig. 5.73. Turn-on time is reduced by increasing forward gate current as in a conventional thyristor, but because the regenerative effect is reduced in the GTO, the gate drive current required for turn-on is larger. To ensure conduction of all cathode fingers and a reduction in on-state voltage, some manufactures recommend a continuous gating current during the entire conduction period.

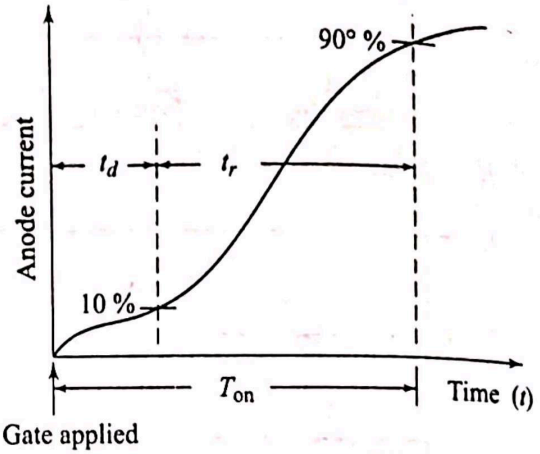


Fig. 5.73 *Delay, rise and turn-on times during gated turn-on*

For high frequency applications, a short turn-on time, especially a short rise time is required to reduce the switching power loss. The power loss dissipated during the delay-time is negligible because of the low anode current.

The GTO is expected to have a faster turn-on time than the conventional thyristor because of its narrower emitter width. The delay time decreases with increasing gate current, while the rise time does not vary so far as the gate current is much smaller than the anode current in the on-state. However, for larger gate drive, the rise time also decreases. The turn-on time also depends upon the rising rate of the gate current; the faster the rising rate, the shorter the turn-on time.

2. *Gate turn-off mechanism* In the conducting state, the central region of the GTO crystal is filled with a conducting electron-hole plasma. To achieve turn-off, excess holes in the *P*-base must be removed by the application of a negative bias to the gate. During the storage phase of the turn-off process, negative gate current extracts excess holes in the *P*-base through the gate terminal. As a result, the anode current path is pinched into a narrow filament under each cathode finger (Fig. 5.71). In this non-regenerative three-layer section of the crystal, current cannot sustain itself and during the full period, the current filaments quickly collapse. Finally, there is a small but slowly decaying tail of anode current due to residual charges in the remoter regions of the crystal.

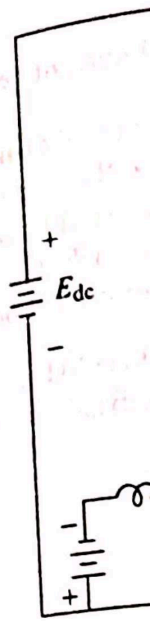


Fig. 5.74 *Basic*

Figure 5.74 shows th
switching circuit with
inductive load. Figure 5
associated voltage
waveforms at turn-off
plified circuit of Fig. 5.
the d.c. supply feeds an
through a series conne
freewheeling diode
across the load to allo
of load current during
of the GTO. The snu
reduces the rate of ri
voltage at turn-off, ther
the current interrupt ca
GTO and also limitin
losses in the device.

Assume the GTO
steady load current, I_a
turn-off is initiated at
and cathode. A rever
inductance of the gate
the storage time T_s. A
tail, current during t
snubber capacitance,

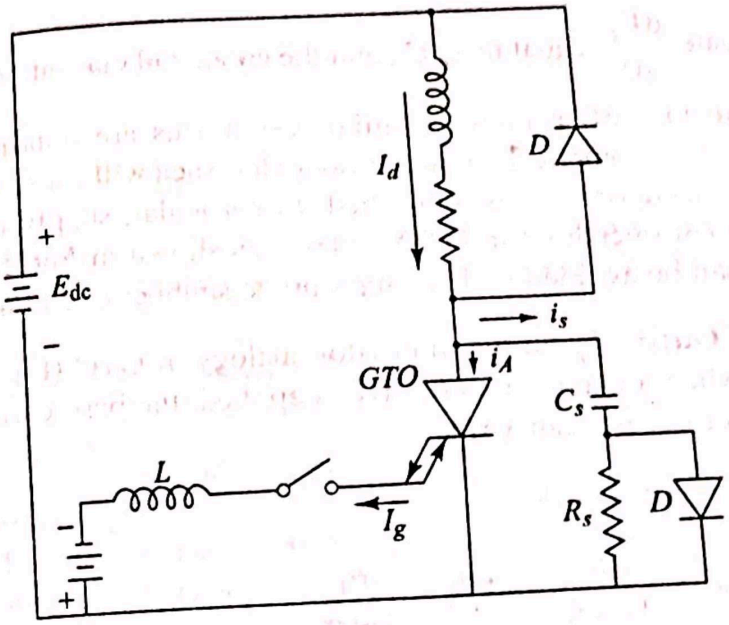


Fig. 5.74 *Basic GTO switching circuit with a clamped inductive load*

Figure 5.74 shows the basic GTO switching circuit with a clamped inductive load. Figure 5.75 shows the associated voltage and current waveforms at turn-off for the simplified circuit of Fig. 5.74. As shown, the d.c. supply feeds an inductive load through a series connected GTO. A freewheeling diode is connected across the load to allow circulation of load current during the off-period of the GTO. The snubber capacitor reduces the rate of rise of forward voltage at turn-off, thereby improving the current interrupt capability of the GTO and also limiting the turn-off losses in the device.

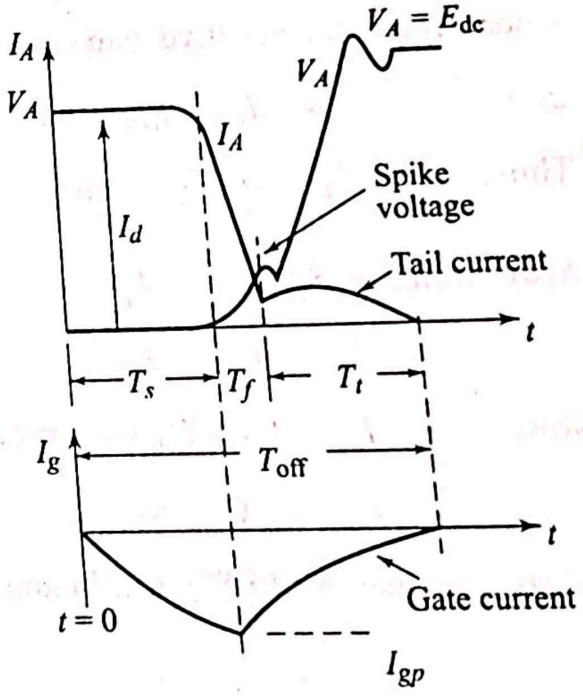


Fig. 5.75 *Voltage and current waveforms during turn-off of a GTO*

Assume the GTO is conducting a steady load current, I_d, when the gate turn-off is initiated at time zero by the application of a reverse bias between gate and cathode. A reverse gate current, I_g, builds up at a rate determined by the inductance of the gate circuit, but the anode current remains constant throughout the storage time T_s. Anode current, I_A, then decreases rapidly to the residual, or tail, current during the fall time, T_f, and the load current is diverted into the snubber capacitance, C_s. As a result, forward voltage, V_A, builds up across the

device at a rate $\frac{dV_A}{dt}$ equal to I_d/C_s, and the anode tail current decays to zero to complete the turn-off process. Similar waveforms are obtained in inverter applications, but in practical circuits, stray inductance will cause some departure from the idealized waveforms described. In particular, supply inductance will cause a transient overshoot in GTO voltage, as shown in Fig. 5.75. Excessive overvoltage can be avoided with an appropriate snubber circuit design.

3. *Turn-off Gain* From two transistor analogy of GTO (Fig. 5.70), we can observe that when a negative gate drive is applied, the base current I_{B2} will be reduced. Therefore, we can write,

$$I_{B2} < I_{C2}/\beta_2 \tag{5.51}$$

where $$\beta_2 = \frac{\alpha_2}{1-\alpha_2} \text{ and } \beta_1 = \frac{\alpha_1}{1-\alpha_1} \tag{5.52}$$

But $$I_{C1} = I_{B2} + I_{GN}$$

where, I_{GN} is the negative gate current.

$$\therefore \quad I_{B2} = I_{C1} - I_{GN}, \text{ but } I_{C1} = \alpha_1 I_{E1}$$

Thus, $$I_{B2} = \alpha_1 \cdot I_{E1} - I_{GN}$$

Also, from Fig. 5.70, $I_{E1} = I_A$

$$I_{B2} = \alpha_1 I_A - I_{GN} \tag{5.53}$$

Now, $$I_{C2} = I_{B2} = I_{E1} - I_{C1} = I_A - \alpha_1 I_A$$

$$I_{C2} = I_A (1 - \alpha_1) \tag{5.54}$$

Substitute equations (5.52), (5.53) and (5.54) in equation (5.51), we get

$$\alpha_1 I_A - I_{GN} < \frac{I_A(1-\alpha_1)}{\alpha_2/(1-\alpha_2)} \quad \therefore \quad \alpha_1 I_A - \frac{I_A(1-\alpha_1)}{\alpha_2/(1-\alpha_2)} < I_{GN}$$

$$\therefore \quad \frac{\alpha_1\alpha_2 I_A - I_A(1-\alpha_1)(1-\alpha_2)}{\alpha_2} < I_{GN}$$

$$\therefore \frac{\alpha_1\alpha_2 I_A - I_A(1-\alpha_2-\alpha_1+\alpha_1\alpha_2)}{\alpha_2} < I_{GN}, \quad \therefore \quad \frac{I_A(\alpha_1+\alpha_2-1)}{\alpha_2} < I_{GN}$$

$$I_{GN} > \frac{I_A}{\alpha_2/(\alpha_1+\alpha_2-1)}$$

$$\therefore \quad \beta_{off} = \frac{\alpha_2}{(\alpha_1+\alpha_2-1)}$$

where,

The parameter β_{off} is known as the tu
clear that to turn-off the GTO, the negati
anode current divided by the turn-off ga

Magnitude of I_{GN} for Reliable Tur

(i) From Eq. (5.56) it is clear that th
depends on the value of turn-off gain
required value of I_{GN}.

(ii) α_1 and α_2 are the transportation
their values are always between 0 and 1.
GTO is of the order 3 to 5. For exam
900 A, then the required negative gate c
to 300 A, which is very high and the co

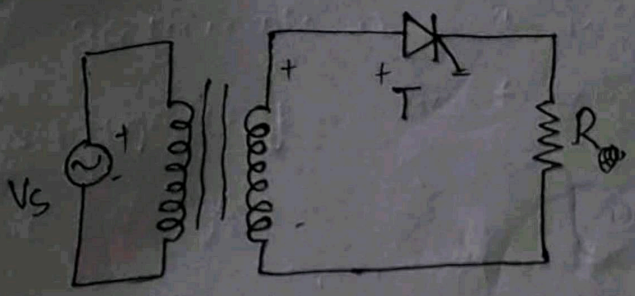
(iii) In GTO, there is always a maxim
If the anode current exceeds this value
off the GTO. If an attempt is made to
which is higher than the maximum co
This is because if anode current is hig
negative gate-current required to turn
cathode junction becomes reverse-bia

5.16.3 GTO Characteristic

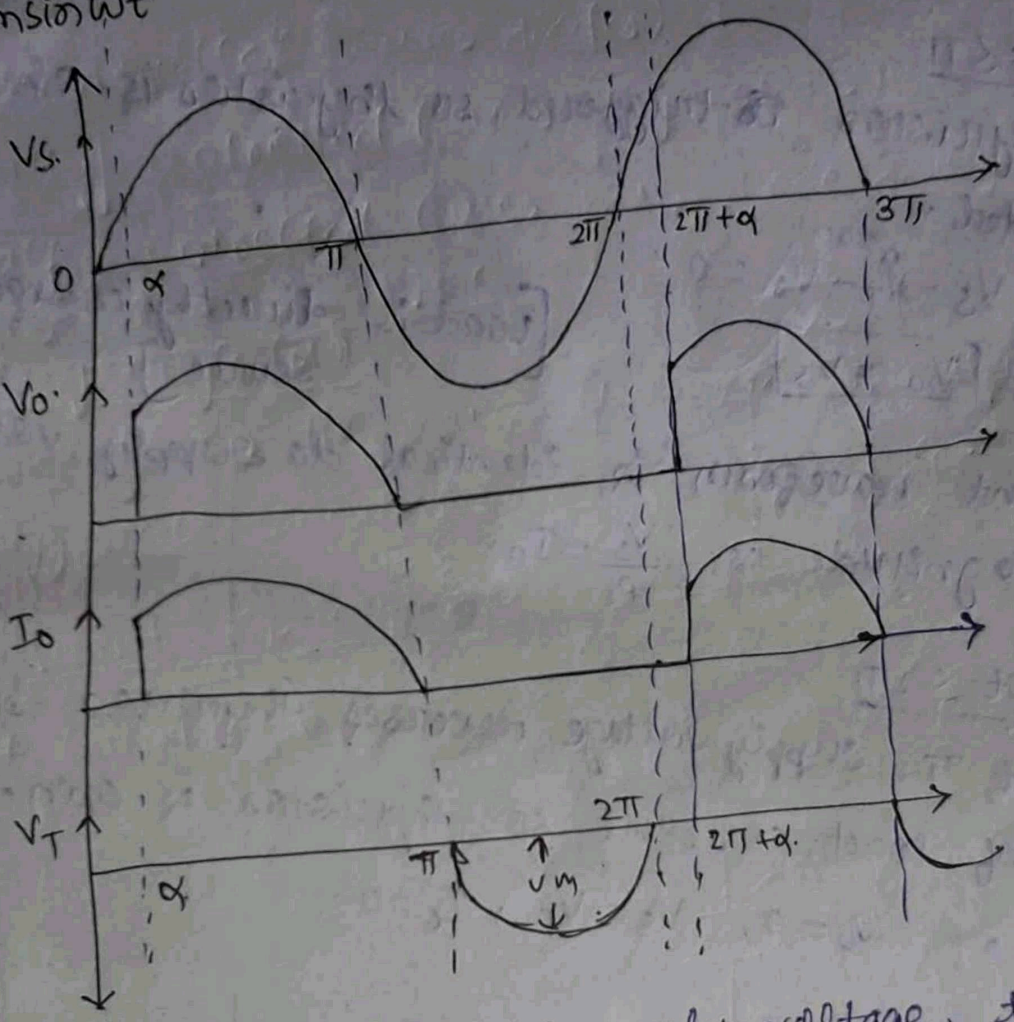
In order to realize the gate-turn-off c
offs are necessary and therefore, sc
those of a conventional thyristor of c
regeneration, there is an increase in la
is also an increase in the on-state vol
a GTO with a shorted anode emitter,
than the forward-blocking voltage b
capability withstand reverse voltag
advantages of the thyristor and has
capability is comparable to that of a co
is possible with a fast semiconduct
cathode structure of the GTO, the di
that in a conventional thyristor. In ge
and large current capability tha
Consequently, the GTO can be used
phase a.c.supplies at 440 V and ab
available, and a single device can b
4500 V and 3500 A.

* 1-ϕ Half wave controlled Converter (with resistive load) :-

Thyristor polarity doesn't changes.



$V_s = V_m \sin \omega t$



During the +ve half cycle of supply voltage, the thyristor anode is +ve w.r.t cathode.

Until the thyristor is triggered it blocks forward current.

Let the triggering angle α, that means thyristor is conducting after α but forward biased from 0 to α.

$0 \le \omega t \le \alpha$

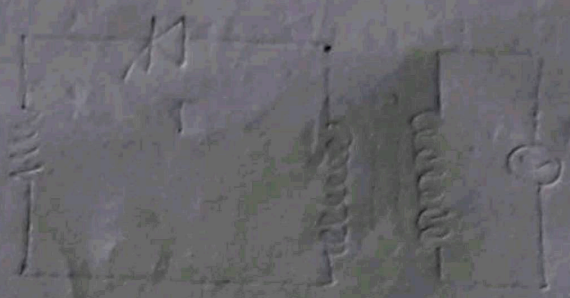
The thyristor is forward biased but not turn on.

So, $V_0 = 0$.

Applying KVL -

$V_S - V_T - \cancel{V_0}^{=0} = 0$

$\Rightarrow \boxed{V_S = V_T}$ $[I_T = I_0 = 0]$



$\alpha \le \omega t \le \pi$

Thyristor ~~is~~ triggered, so thyristor is short circuited.

$V_S - \cancel{V_T}^{=0} - V_0 = 0$

$\Rightarrow \boxed{V_0 = V_S}$ [Load is directly connected to source]

Current waveform is identical to supply voltage & magnitude is $\frac{V_S}{R} = I_0$.

$\pi \le \omega t \le 2\pi$

At π supply voltage reverses, thyristor blocks the flow of load current so, thyristor is open circuited.

So, $V_0 = 0$, $V_S = V_T$, $I_0 = 0$.

$2\pi \le \omega t \le 2\pi + \alpha$

same as $0 \le \omega t \le \alpha$

Average Load voltage :-

$$V_0 = \frac{1}{2\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d\omega t$$

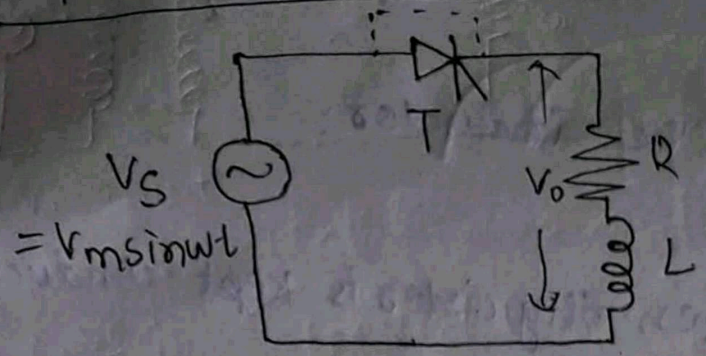
$$= \frac{V_m}{2\pi} \left[-\cos \omega t \right]_{\alpha}^{\pi}$$

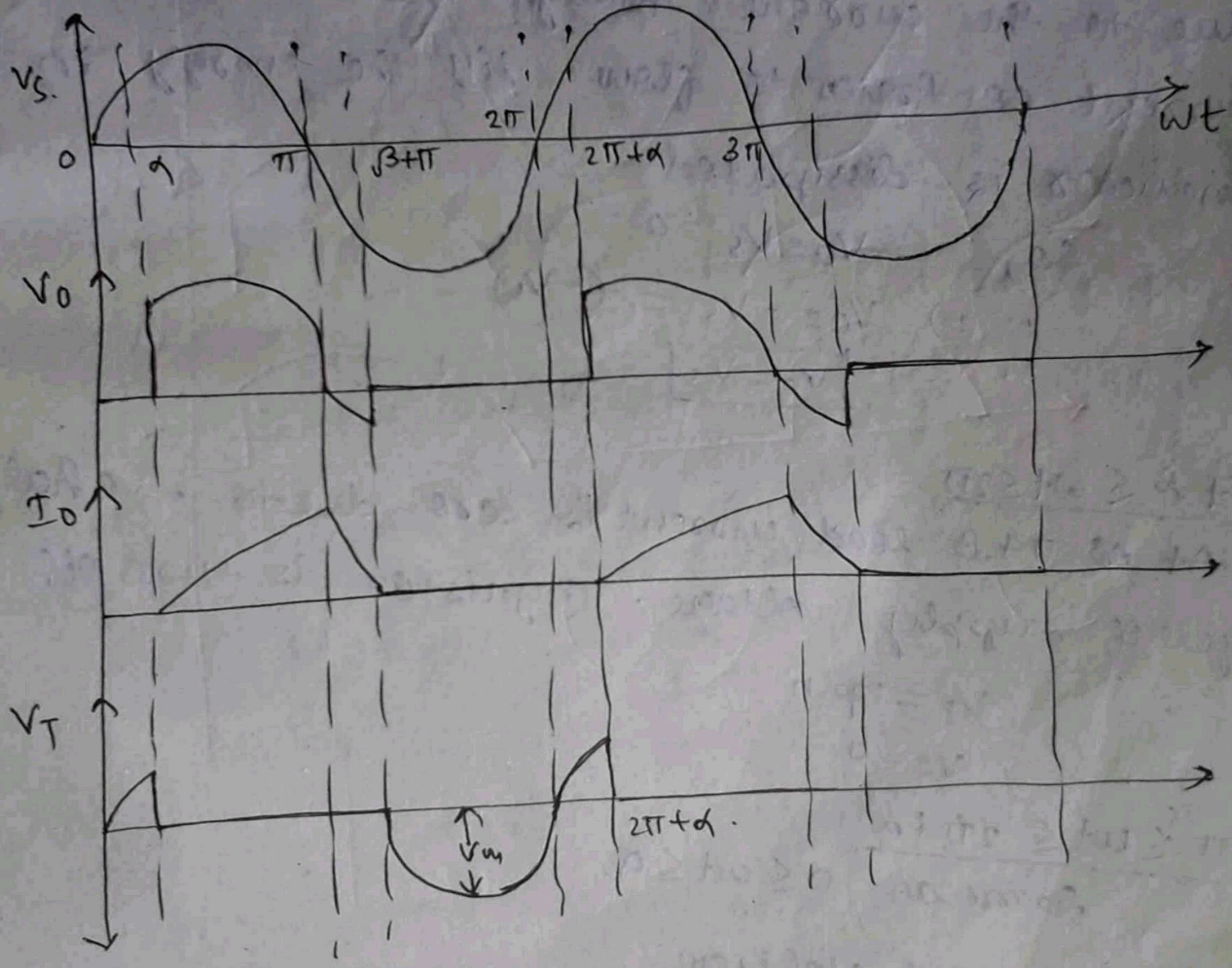
$$= -\frac{V_m}{2\pi} \left[\cos \pi - \cos \alpha \right].$$

$$V_o' = \frac{V_m}{2\pi}(1+\cos\alpha)$$

$$\text{So, } I_o = \frac{V_o}{R} = \frac{V_m(1+\cos\alpha)}{2\pi R}$$

* 1-ϕ Half wave Rectifier with R-L Load





$0 \le \omega t \le \alpha$

Thyristor is not triggered so ckt is open.

$V_o = 0$.

$V_S = V_T$.

$I_o = 0$.

$\alpha \leq \omega t \leq \pi$

Thyristor is triggered, the load current will increase in a finite time to the inductive load.

$$V_S - \cancel{V_T}^{=0} - V_O = 0 \qquad \left[\text{As } V_T = 0 \text{ s.c}\right]$$

$$\Rightarrow \boxed{V_S = V_O}$$

Energy stored in the inductor.

$\pi \leq \omega t \leq \pi + \beta$

Supply voltage reverses, thyristor is kept conducting due to the current through the inductance. The current continues to flow till the energy in the inductor is dissipated.

$$\text{So,} \quad -V_O - V_S = 0$$

$$\Rightarrow V_O = -V_S = -(-V_S)$$

$$\Rightarrow \boxed{V_O = V_S}$$

$\pi + \beta \leq \omega t \leq 2\pi$

At $\pi + \beta$ load current is zero due to -ve half cycle of supply voltage. Thyristor is turn off.

$$V_T = \text{Open}$$

$$V_O = 0$$

$2\pi \leq \omega t \leq 2\pi + \alpha$

Same as $0 \leq \omega t \leq \alpha$.

Average Load voltage:-

$$V_{Oavg} = \frac{1}{2\pi} \int_{\alpha}^{\pi+\beta} V_m \sin \omega t \, d\omega t$$

$$= \frac{V_m}{2\pi} \left[-\cos \omega t\right]_{\alpha}^{\pi+\beta}$$

$$= -\frac{V_m}{2\pi}\left[\cos(\pi+\beta) - \cos\alpha\right].$$

$$= -\frac{V_m}{2\pi}\left[\cos\pi\cos\beta - \sin\pi\sin\beta - \cos\alpha\right].$$

$$= -\frac{V_m}{2\pi}\left[-\cos\beta - \cos\alpha\right].$$

$$V_{o\,avg} = \frac{V_m}{2\pi}\left(\cos\alpha + \cos\beta\right).$$

And, $I_{o\,avg} = \frac{V_o}{R} = \frac{V_m(\cos\alpha + \cos\beta)}{2\pi R}$.

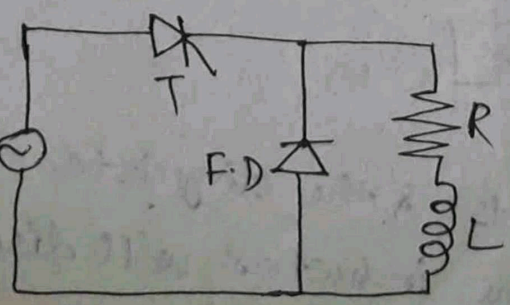
→ **Effect of Load Inductance**

(i) The average o/p voltage decreases.

(ii) The load current wave form is discrete (mixture of exponential & sinusoidal).

→ **Effect of Free Wheeling Diode :-**

By using free wheeling diode, we can improve the average o/p voltage. -ve half cycle of o/p voltage comes due to the inductor can't dissipate its energy during time period α to π completely so, it takes some extra time ie., π to $\pi+\beta$. The demerit of inductive load can be improved by using a diode across the load which is known as free wheeling diode.



to the path, $V_0 \rightarrow D \rightarrow V_0$ $(L \rightarrow D \rightarrow R_0 \rightarrow L)$

So, $-V_0 - V_D = 0$ $\because [V_D = SC]$

$\Rightarrow \boxed{V_0 = 0}$

* In this time free-wheeling action takes place & no power will transfer to the source.

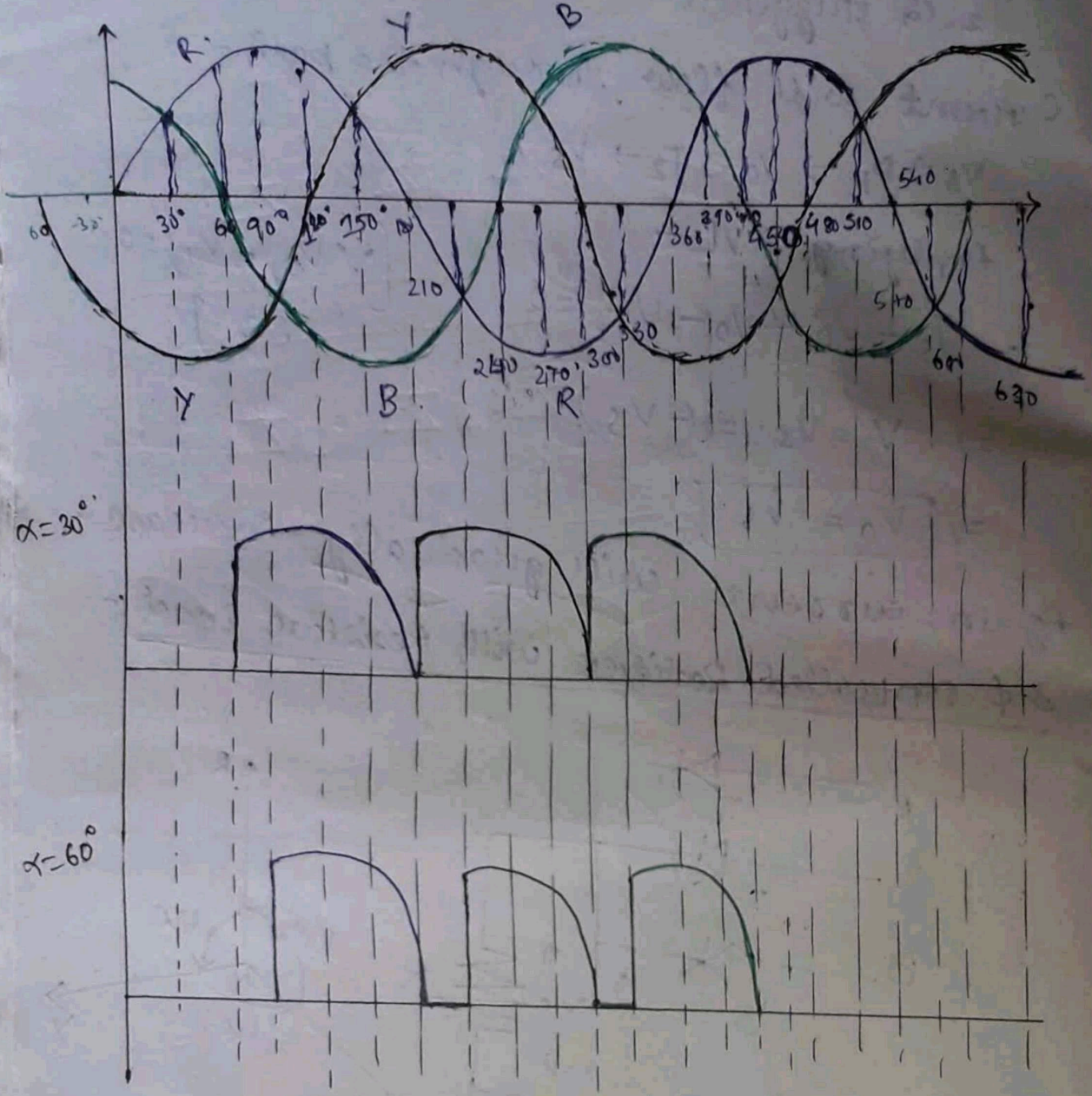
$\pi + \beta \leq \omega t \leq 2\pi$

All energy of inductor is dissipated and ckt is open, So, $V_0 = 0$, $V_T = V_s$ (supply -ve)

$$V_s + V_T = 0$$
$$\Rightarrow V_T = -V_s$$
$$\Rightarrow V_T = -(V_s) = V_s$$
$$\Rightarrow \boxed{V_T = V_s}$$

point converter

$[\omega t = 30^\circ + \alpha]$

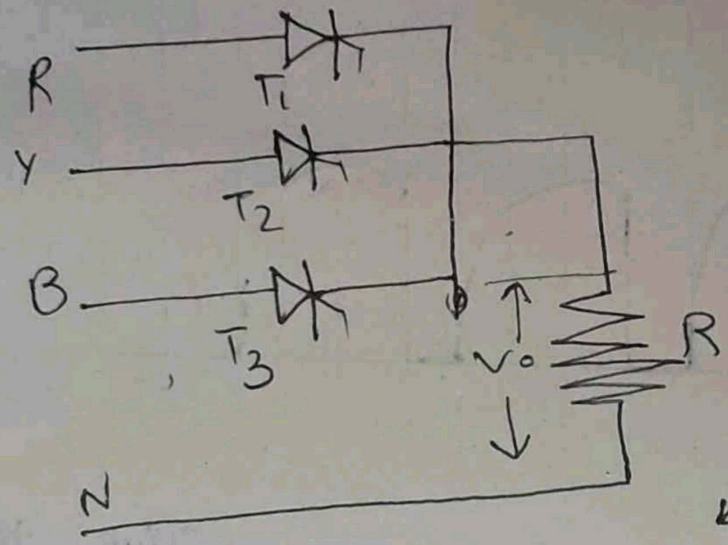


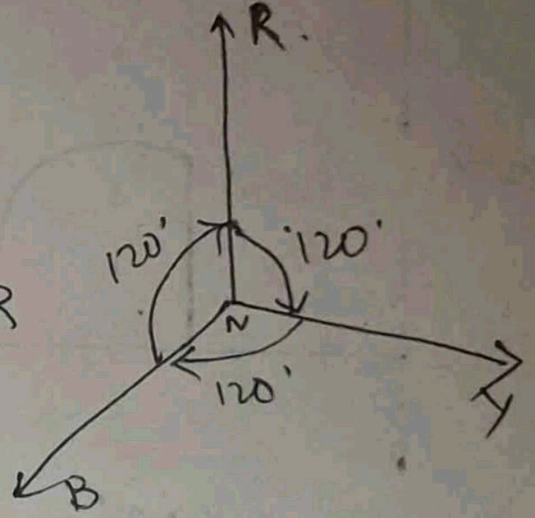
$30^\circ \leq \omega t \leq 150^\circ$

At ~~$\omega t = 030^\circ$~~, as R is more positive than B. So, T_1 is forward biased but not triggered. As, $\boxed{\alpha = 30^\circ}$, so, the T_1 is triggered at $\omega t = 60^\circ$. So, T_1 will conduct & the current will flow through path, $R \rightarrow V_{T_1} \rightarrow R \rightarrow N$

Again, current will g...

* 3-ϕ Controlled Rectifier with Resistive Load :-





$V_R = V_m \sin \omega t$

$V_Y = V_m \sin(\omega t - 120^\circ)$

$V_B = V_m \sin(\omega t - 240^\circ) = V_m \sin(\omega t + 120^\circ)$

At ~~wt 150°~~ $150° \leq wt \leq 180°$

Although, Y is more positive than R but T_2 will not conduct since T_2 is not triggered. ~~but~~ So, the output will come due to thyristor T_1.

At ~~wt=180°~~ $180 \leq wt \leq 300°$

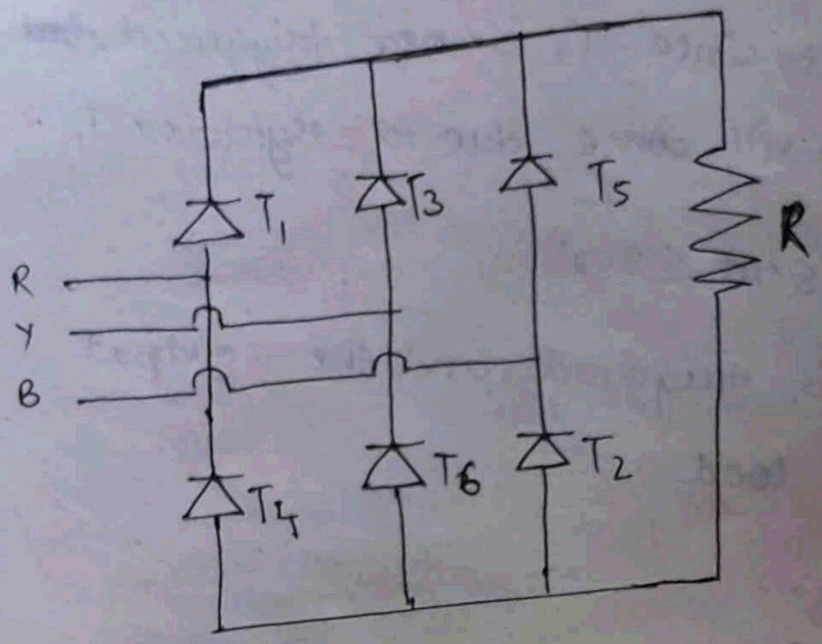
Thyristor T_2 is triggered and the output appears at the load.

At $300 \leq wt \leq 330°$

The thyristor T_2 will conduct upto ~~300°~~ $wt = 300°$ although B is more positive than Y. At $wt = 300°$ T_3 becomes forward biased but not triggered. So, ~~after~~ at $wt = 330°$, T_3 is triggered and conducts and the output comes due to T_3.

* The output can be controlled by triggering the thyristors at different firing angles 'α'.

* 3-ϕ 6-Pulse Converter (with R-Load)



T_2, T_4 & T_6 are negative groups. T_1, T_3 & T_5 are positive groups. The firing gap between group member is 120°. The firing gap between arm member is 180°.

$V_R = V_m \sin \omega t$

$V_Y = V_m \sin(\omega t - 120^\circ)$

$V_B = V_m \sin(\omega t - 240) = V_m \sin(\omega t + 120^\circ)$

At, $120 \leq \omega t \leq 180^\circ$

Thyristors 1 & 2 are conducting.

So, ~~applying KVL~~ current flows through the path -

$V_R \rightarrow T_1 \rightarrow V_0 \rightarrow T_2 \rightarrow V_B$

Applying KVL –

$$V_R - \cancel{V_{T_1}^{=0}} - V_0 - \cancel{V_{T_2}^{=0}} - V_B = 0$$

$$\Rightarrow \boxed{V_0 = V_R - V_B}$$

Now, $V_R = V_m \sin \omega t$

$V_B = V_m \sin(\omega t + 120^\circ)$

So, $V_0 = V_R - V_B$

$= V_m \sin \omega t - V_m \sin(\omega t + 120^\circ)$

Now, At $\omega t = 120^\circ$

$V_0 = V_m \sin 120^\circ - V_m \sin(120^\circ + 120^\circ)$

$= \frac{V_m \sqrt{3}}{2} - \left(-\frac{V_m \sqrt{3}}{2}\right)$

$= \frac{2 V_m \sqrt{3}}{2}$

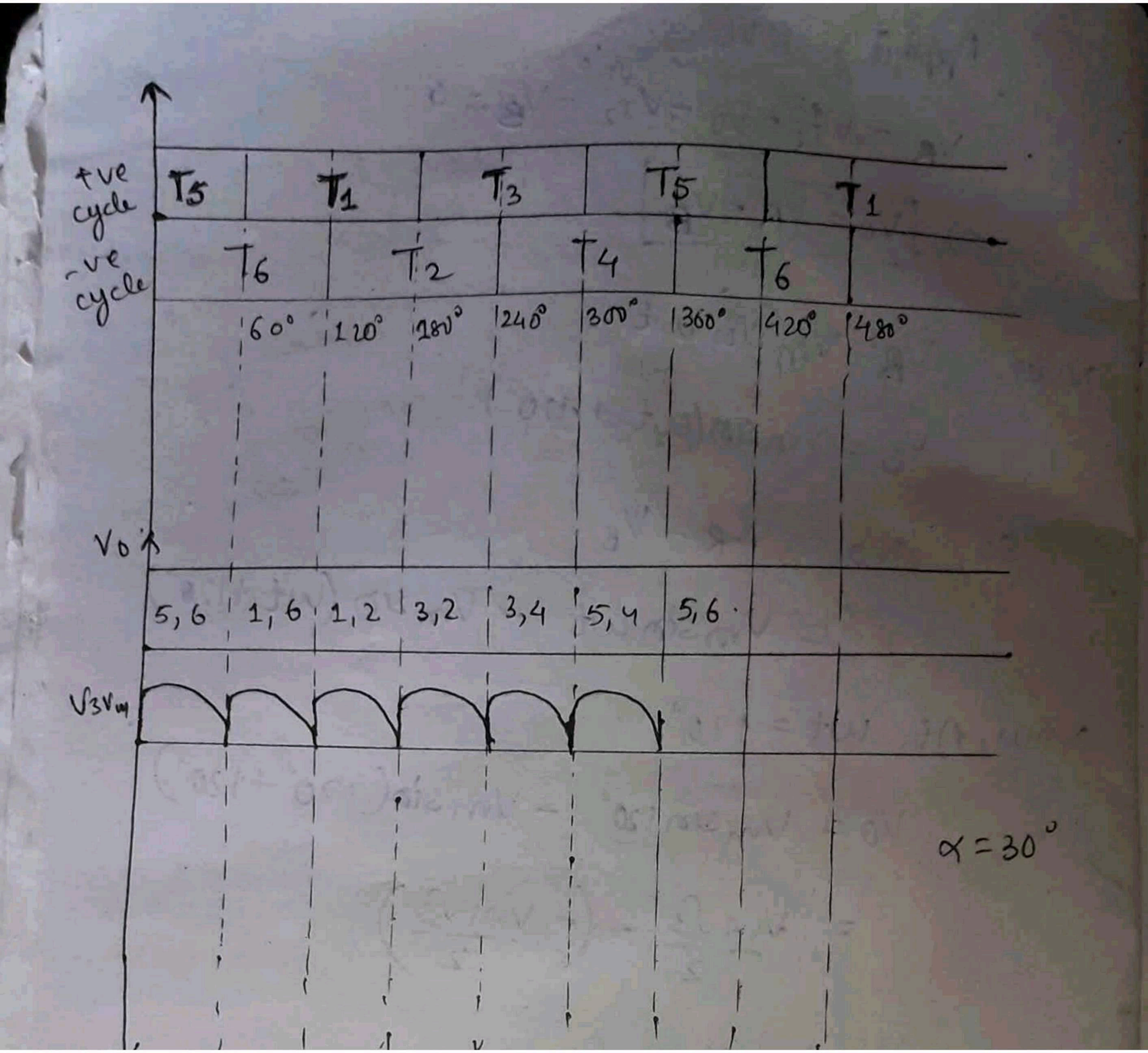
$$\boxed{V_0 = \sqrt{3} V_m}$$

At $\omega t = 180^\circ$

$V_0 = V_m \sin 180^\circ - V_m \sin(180^\circ + 120^\circ)$

$= 0 - \left(-\frac{\sqrt{3}}{2} V_m\right)$

$$\Rightarrow \boxed{V_0 = \frac{\sqrt{3}}{2} V_m}$$


+ve cycle
-ve cycle
T5
T1
T3
T5
T1
T6
T2
T4
T6
60°
120°
180°
240°
300°
360°
420°
480°
Vo
5,6
1,6
1,2
3,2
3,4
5,4
5,6
V3Vm
α = 30°

30/08/17

CHOPPER

Its a power electronic device which converts fixed DC to variable DC.

It is simple switching device where MOSFET, IGBT, BJT, GTO are used for switching device.

It is used in electrical drives (speed control of DC motor.

There are two types of chopper -

→ AC link chopper ⇒ DC → [Inverter] → AC → [converter] → DC (modified)

→ DC link chopper ⇒

* Classifications of Chopper according to Quadrant Operation

(1) Type - A

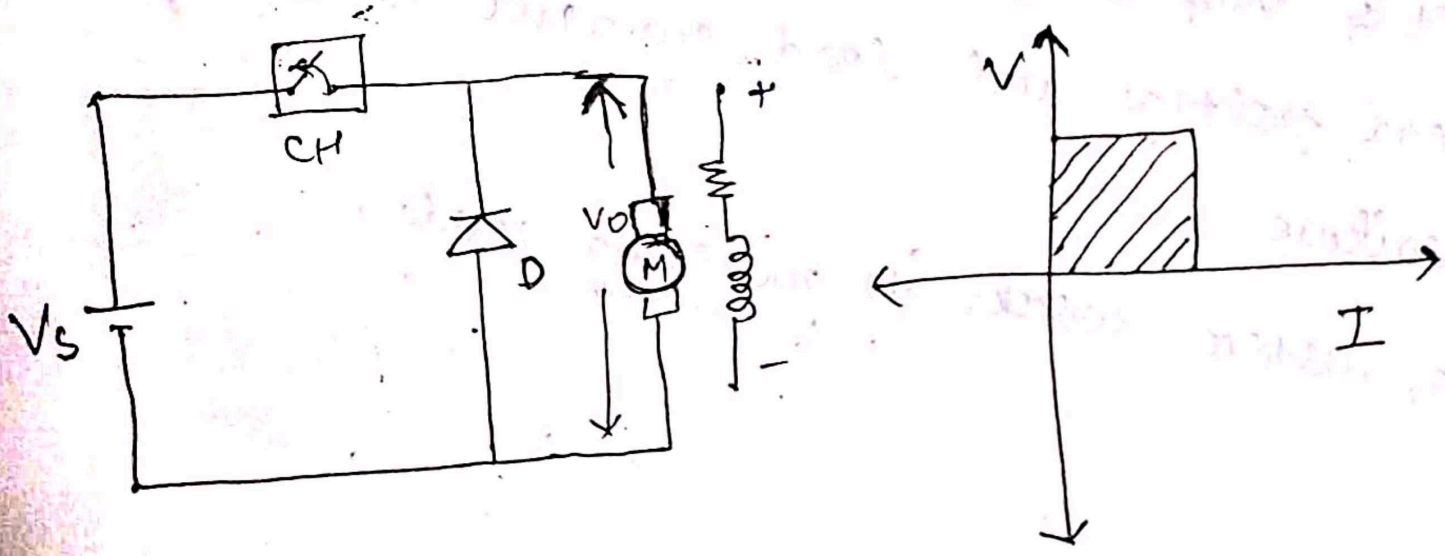
(2) Type - B

(3) Type - C

(4) Type - D

(5) Type - E

* Type - A chopper (First Quadrant



When chopper is ON, the source current will flow through the path, $V_s \rightarrow CH \rightarrow M \rightarrow V_s$.

Applying KVL –

$$V_S - \cancel{V_{CH}}^{=0} - V_O = 0$$

$$\Rightarrow \boxed{V_O = V_S} \quad \text{i.e., } I_O = +ve.$$

$$\Rightarrow V_O = +V_S.$$

In this case, the current direction is taken as positive.

When chopper is OFF; Inductor will release its energy in the path;

$$M \rightarrow F.D \rightarrow M.$$

Applying KVL –

$$-V_O - \cancel{V_D}^{=0} = 0.$$

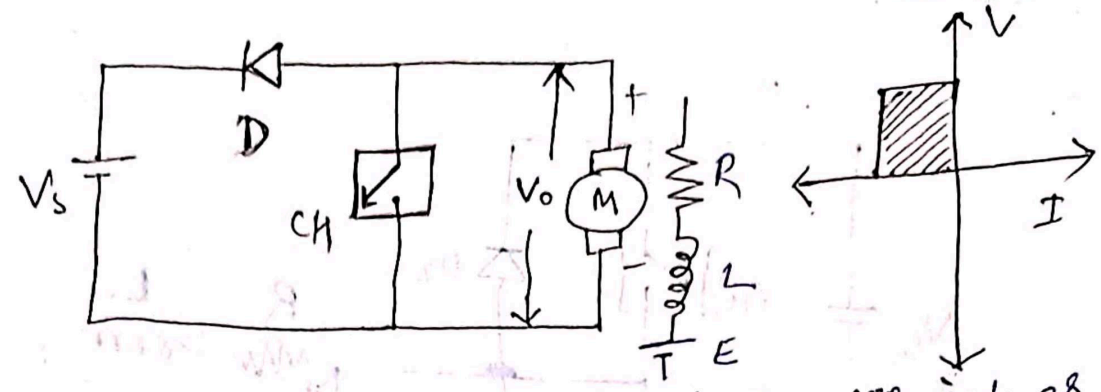
$$\Rightarrow V_O = 0 \text{ (but is positive)}.$$

Current flows in the same direction as previous i.e., I_O is positive.

It is thus seen that average value of both load voltage and load current is always positive.

So, motor works in motoring mode.

* Type-B Chopper (Second Quadrant)



When chopper is ON, the emf E will act as a DC source, so, the load current will flow through the path,

M → CH → M.

↓ = I = +ve

↑ = I = -ve.

Applying KVL -

$V_o - V_{CH} = 0$ ($V_{CH} = 0$)

$\Rightarrow V_o = 0$, $I_o = -ve$

This time inductor will stores its energy.

Again, when chopper is OFF, $E + L\frac{di}{dt} > V_s$ diode 'D' is forward biased and the load current will flow through the path -

M → D → Vs → M

Applying KVL -

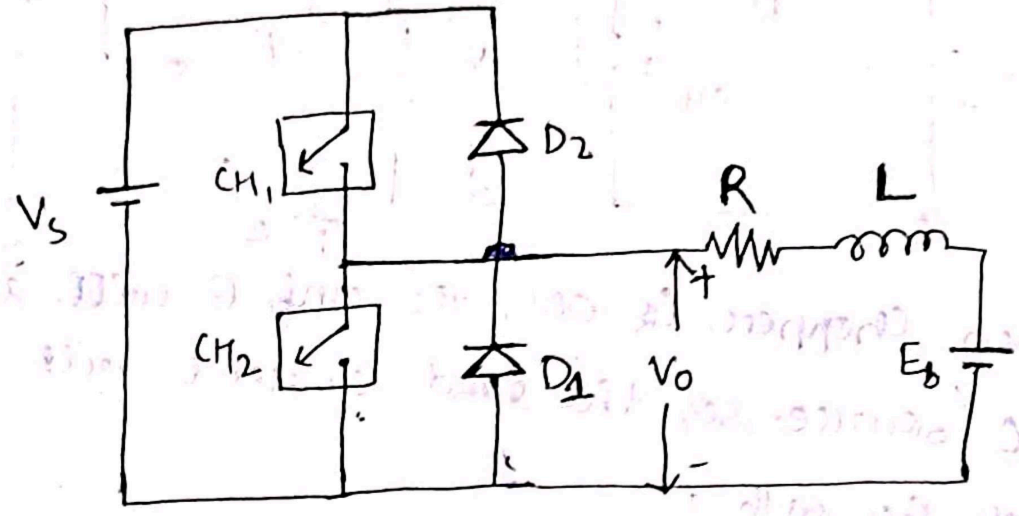
$V_o - V_D - V_s = 0$ ($V_D = 0$)

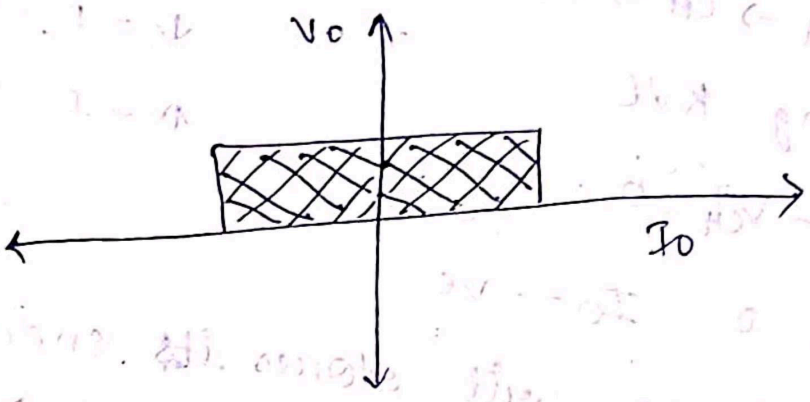
$\Rightarrow V_o = V_s$ & $I_o = -ve$.

So, V_o is always positive & I_o is always negative.

This is called regenerative braking mode.

* Type-C Chopper :-





When CH1 is ON, current will flow through

path - $V_s \rightarrow CH1 \rightarrow R \rightarrow L \rightarrow E_b \rightarrow V_s$

Applying KVL -

$$V_s - \cancel{V_{CH1}}^{=0} - V_o = 0$$

[I_o is assumed as +ve].

$\Rightarrow V_o = V_s = +ve$, $I_o = +ve$

In this time, inductor will stores its energy (with left positive & right negative)

when CH_1 is OFF, inductor will dissipate its energy (with left negative & right positive) which will forward bias the diode D_1, so the current will flow through path,

$$L \to E_b \to D_1 \to R \to L$$

Applying KVL -

$$-V_0 - V_{D_1}^{=0} = 0$$

$$\Rightarrow V_0 = 0 \quad \& \; I_0 = +ve$$

current will gradually increase.

Again, when $E_b > L\frac{di}{dt}$ and CH_2 is ON which will forward bias the CH_2, current will flow through path -

$$E_b \to L - R \to CH_2 - E_b$$

$$V_0 - V_{CH_2}^{=0} = 0$$

$$\Rightarrow V_0 = 0, \; I_0 = -ve$$

In this time inductor will stores its energy (with right plate +ve & left plate -ve).

when CH_2 is OFF, ~~$E_b + L\frac{di}{dt}$~~ inductor will release its energy (with right plate -ve & left plate +ve)

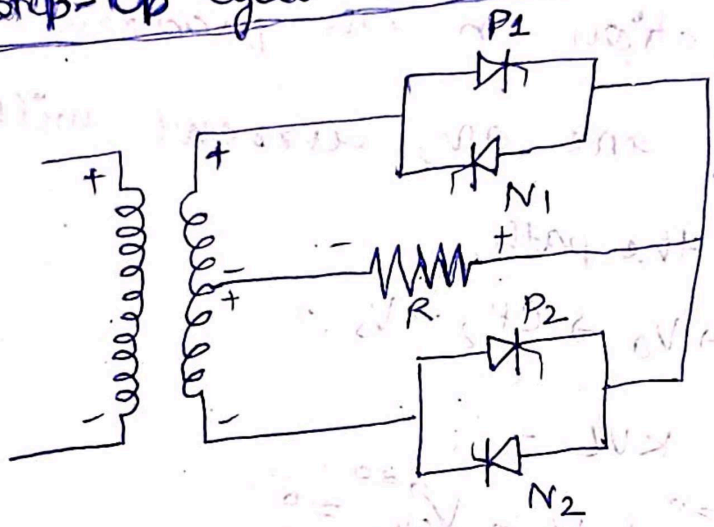
when, $E_b + L\frac{di}{dt} > V_S$, diode D_2 will forward bias, then load current will flow through path -

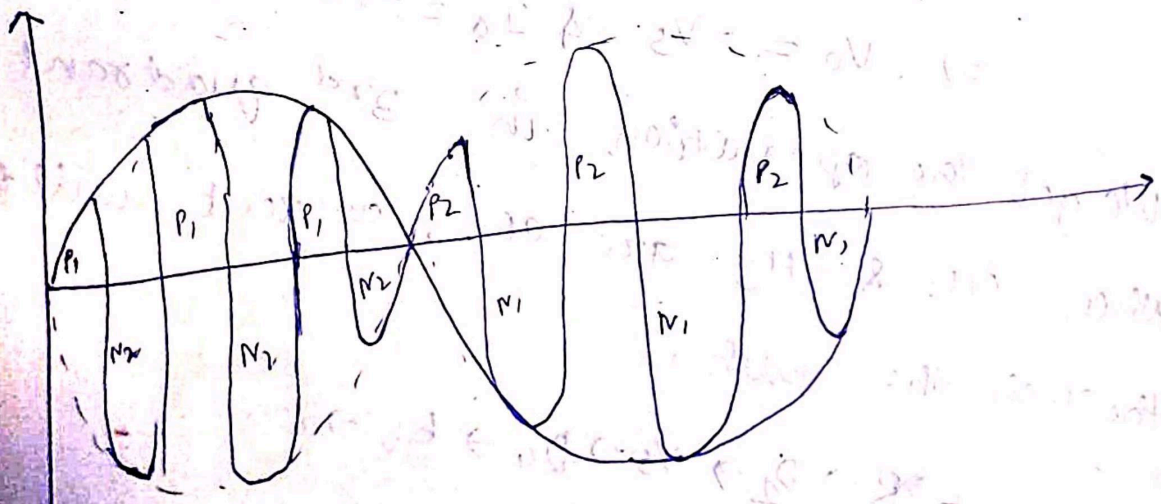
$$E_b - L - R - D_2 - V_S - E_b$$

* Cyclo-Converter :-

A cyclo-converter is a type of power controller in which an alternating voltage at supply frequency is converted to an alternating voltage of load frequency.

→ Step-Up Cyclo Converter (Mid-point type)





$0 \leq \omega t \leq \pi$

+ve half cycle starts, P_1 & N_2 are forward biased

At $\omega t = 0$, P_1 is triggered, so, current will flow through the path,

$$V_S \rightarrow P_1 \rightarrow V_0 \rightarrow V_S$$

Applying KVL -

$$V_S - \cancel{V_{P_1}^{=0}} - V_0 = 0$$

$$\Rightarrow \boxed{V_0 = V_S}$$

At $\omega t = \omega t_1$, P_1 is forcefully turned OFF and N_2 will be triggered, so, current will flow through the path -

$$V_S \rightarrow V_0 \rightarrow N_2 \rightarrow V_S$$

Applying KVL -

$$V_S + V_0 - \cancel{V_{N_2}^{=0}} = 0$$

$$\Rightarrow \boxed{V_0 = -V_S}$$

At $\omega t = \omega t_2$, N_2 is forcefully turned OFF and P_1 will be triggered.

Again, load current will flow through the path -

$$V_S \rightarrow P_1 \rightarrow V_0 \rightarrow V_S$$

Applying KVL -

$$V_S - \cancel{V_{P_1}^{=0}} - V_0 = 0$$

$$\Rightarrow \boxed{V_0 = V_S}$$

At $wt = wt_3$:-

P_1 will be forcefully turned OFF and N_2 will be triggered. So, current will flow through the path -

$V_s \rightarrow V_o \rightarrow N_2 \rightarrow V_s$.

Applying KVL -

$V_s + V_o - \cancel{V_{N_2}}^{=0} = 0$

$\Rightarrow \boxed{V_o = -V_s}$

At $wt = wt_4$

P_1 will be turned ON and N_2 is forcefully turned OFF. So, current will flow through the path -

$V_s \rightarrow P_1 \rightarrow V_o \rightarrow V_s$

Applying KVL -

$V_s - \cancel{V_{P_1}}^{=0} - V_o = 0$

$\Rightarrow \boxed{V_o = V_s}$

At $wt = wt_5$

P_1 will be forcefully turned OFF and N_2 will be turned ON. So, current will flow through the path -

$V_s \rightarrow V_o \rightarrow N_2 \rightarrow V_s$

Applying KVL -

$V_s + V_o - \cancel{V_{N_2}}^{=0} = 0$

$\Rightarrow \boxed{V_o = -V_s}$

At $\omega t = \pi$

-ve half cycle starts, N_1 and P_2 are forward biased.

P_2 is triggered. So, current will flow through the path –

$$V_s \rightarrow P_2 \rightarrow V_o \rightarrow V_s$$

Applying KVL –

$$V_s - \cancel{V_{P_2}}^{=0} - V_o = 0$$

$$\Rightarrow \boxed{V_o = V_s} \Rightarrow V_o = -V_s \Rightarrow \boxed{V_o = -V_s}$$

At $\omega t = \omega t_6$

P_2 will be forcefully turned OFF & N_1 will be turned on. So, current flows through path –

$$V_s \rightarrow V_o \rightarrow N_1 \rightarrow V_s$$

Applying KVL –

$$V_s + V_o - \cancel{V_{N_1}}^{=0} = 0$$

$$\Rightarrow V_o = -V_s = -(-V_s)$$

$$\Rightarrow \boxed{V_o = V_s}$$

At $\omega t = \omega t_7$

P_2 will be triggered & N_1 will be forcefully turned OFF. So, current will flow through the path –

$$V_s \rightarrow P_2 \rightarrow V_o \rightarrow V_s$$

Applying KVL –

$$V_s - \cancel{V_{P_2}}^{=0} - V_o = 0$$

$$\Rightarrow V_o = V_s = (-V_s) \Rightarrow \boxed{V_o = -V_s}$$

At $\omega t = \omega t_8$

N_1 will be triggered and P_2 will be forcefully turned OFF. So, current flows through the path -

$V_s \rightarrow V_0 \rightarrow N_1 \rightarrow V_s$

Applying KVL -

$V_s + V_0 - \cancel{V_{N_1}}^{=0} = 0$

$\Rightarrow V_0 = -V_s$

$\Rightarrow V_0 = -(-V_s) \Rightarrow \boxed{V_0 = V_s}$

At $\omega t = \omega t_9$

P_2 will be triggered and N_1 will be forcefully turned OFF. So, current flows through the path -

$V_s \rightarrow P_2 \rightarrow V_0 \rightarrow V_s$

Applying KVL -

$V_s - \cancel{V_{P_2}}^{=0} - V_0 = 0$

$\Rightarrow V_0 = V_s \Rightarrow V_0 = -(+V_s)$

$\Rightarrow \boxed{V_0 = -V_s}$

At $\omega t = \omega t_{10}$

N_1 will be triggered and P_2 will be forcefully turned OFF. So, current flows through the path -

$V_s \rightarrow V_0 \rightarrow N_1 \rightarrow V_s$.

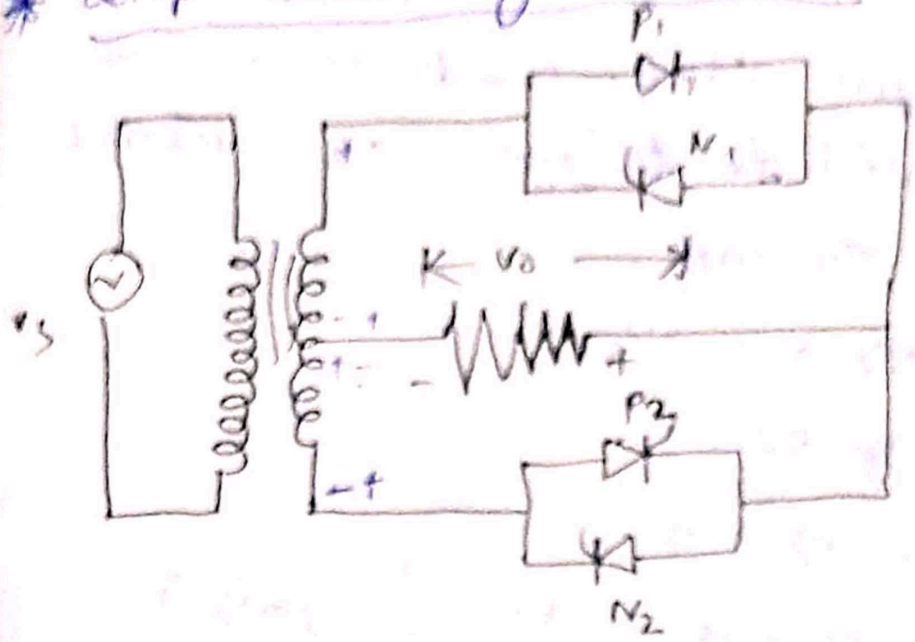
Applying KVL -

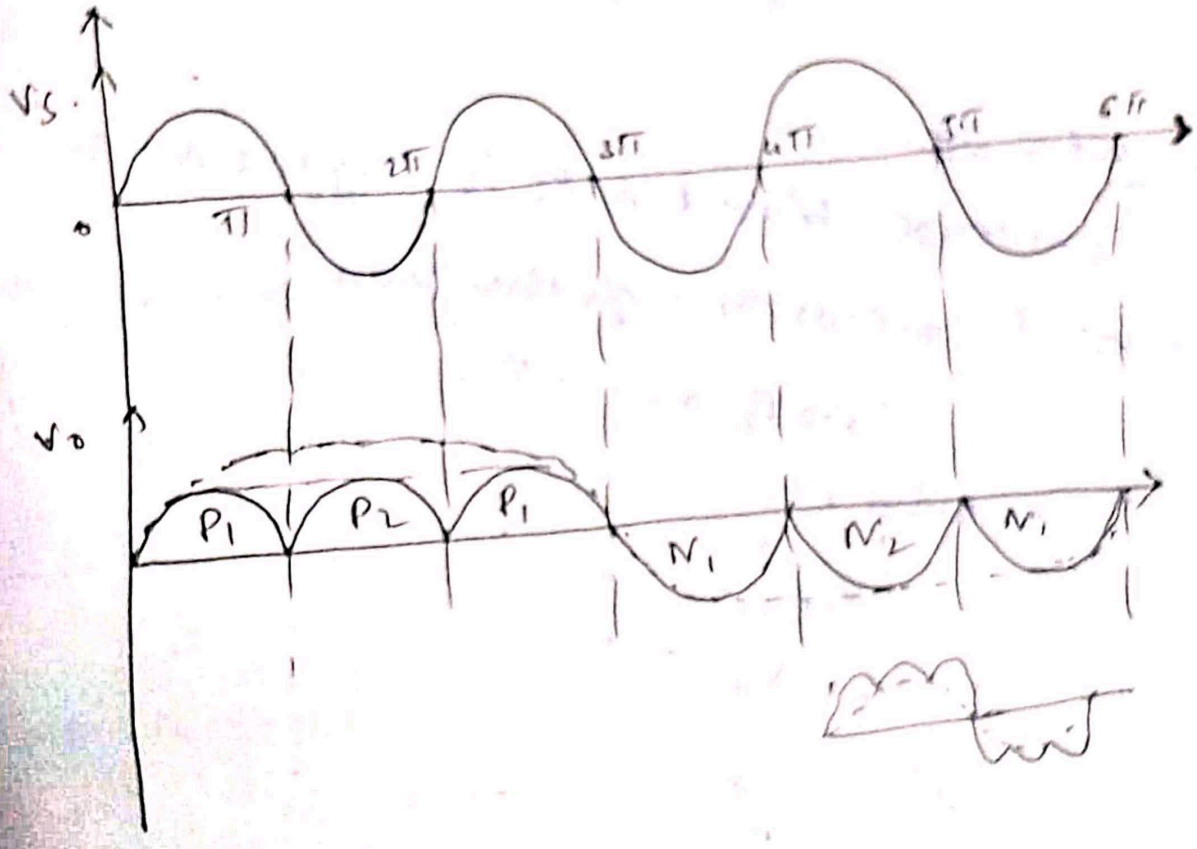
$V_s + V_0 - \cancel{V_{N_1}}^{=0} = 0$

$\Rightarrow V_0 = -V_s \Rightarrow V_0 = -(-V_s)$

$\Rightarrow \boxed{V_0 = V_s}$

* Step-down Cycloconverter





At $0 \le \omega t \le \pi$

+ve half cycle starts, Thyristors P_1 is triggered.

So, current flows through the path.

$V_s \rightarrow P_1 \rightarrow V_o \rightarrow V_s$.

Applying KVL -

$V_s - \overset{=0}{V_{P_1}} - V_o = 0 \quad \Rightarrow \boxed{V_o = V_s}$

VSI

(i) We can provide a constant voltage by connecting a capacitor across the voltage source.

(ii) Source impedance is negligible.

(iii) Feedback diode is present so any device can be used as switch.

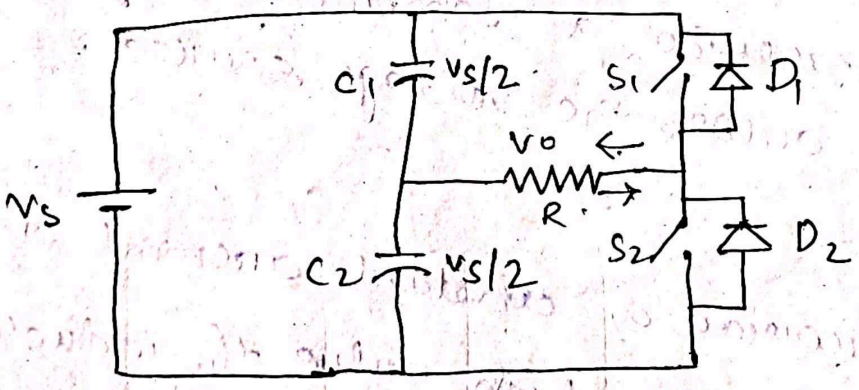
CSI

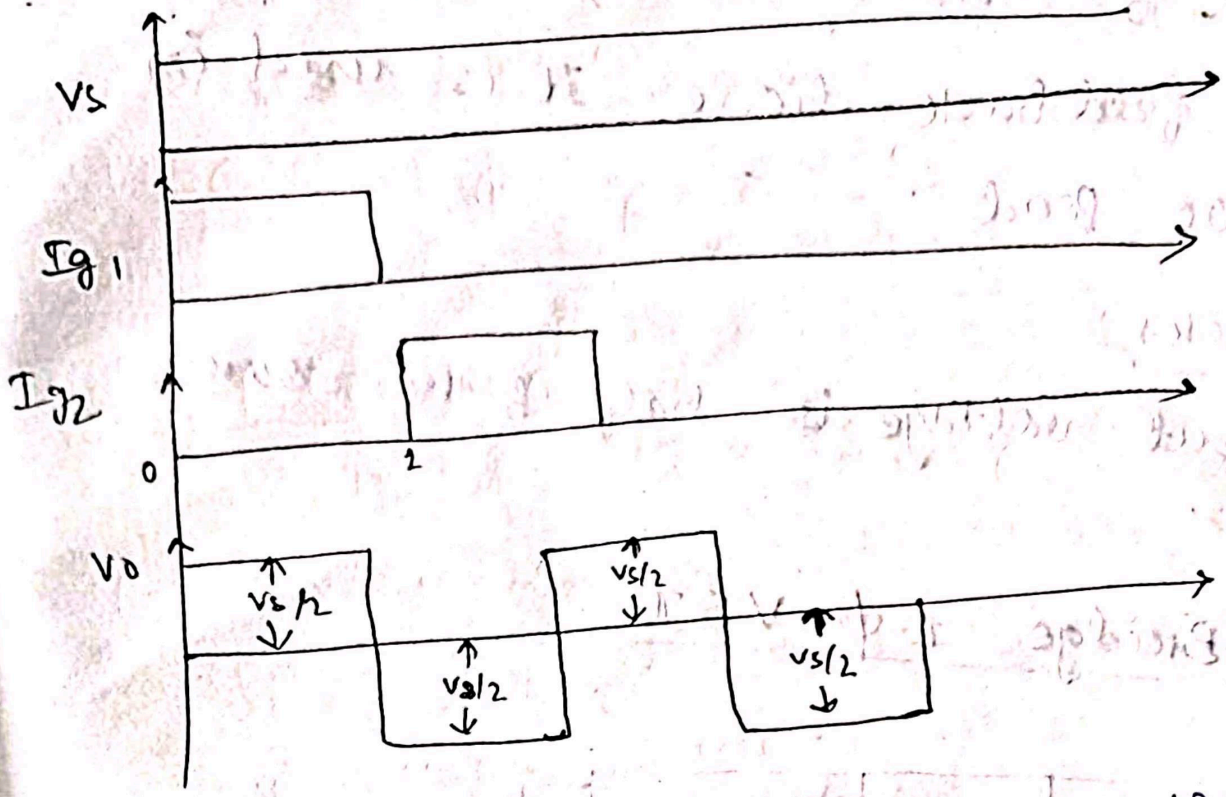
(i) We can provide a constant current by providing a series high value of inductance with the voltage source.

(ii) Source impedance is very high.

(iii) Feedback diode is absent so the device like MOSFET & BJT cannot be used because it cannot withstand like reverse voltage.

* Half Bridge 1-ϕ VSI





When S_1 is closed, current flows through the path,

$$V_{s/2} \rightarrow S_1 \rightarrow V_0 \rightarrow V_{s/2}$$

So, the output voltage is -

$$V_{s/2} - V_{s_1}^{=0} - V_0 = 0$$

$$\Rightarrow \boxed{V_0 = \frac{V_s}{2}}$$

When S_1 is turned OFF and S_2 is turned ON then load current will flow through the path -

$$V_{s/2} \rightarrow V_0 \rightarrow S_2 \rightarrow V_{s/2}.$$

So, the output voltage is -

$$V_{s/2} + V_0 - V_{s_2}^{=0} = 0$$

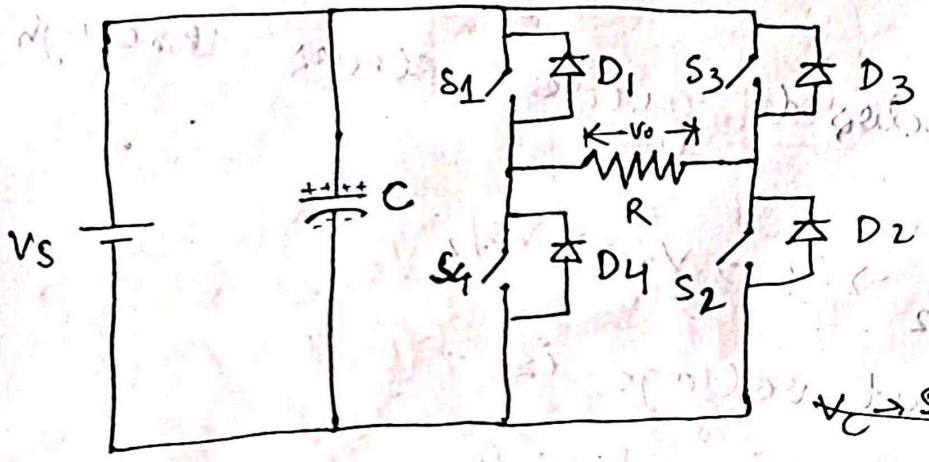
$$\Rightarrow \boxed{V_0 = -V_{s/2}}$$

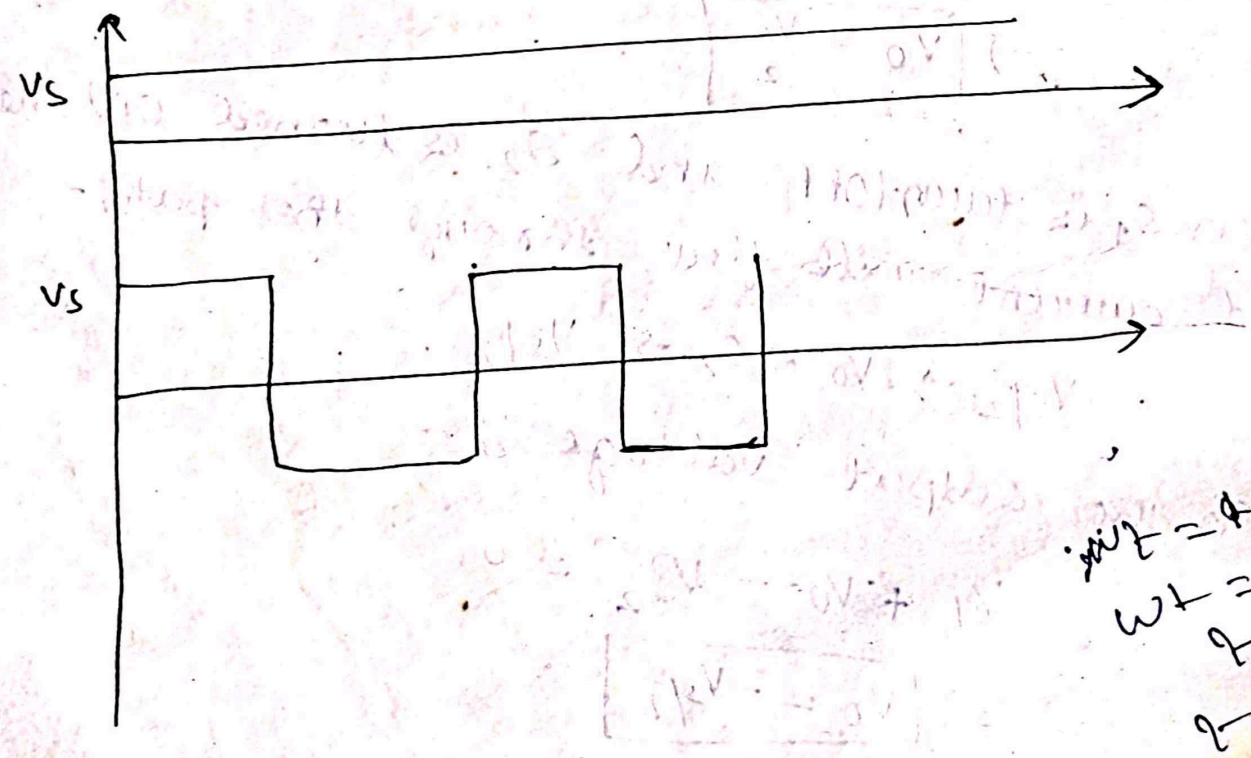
* In case of resistive load, there is no use of feedback diode. It is used in inductive load.

→ Drawbacks :-

(i) output voltage is half of the source voltage.

* Full Bridge 1-ϕ, VSI





ωt = π
ωt = π

capacitor is charged to a voltage V_s. when switch S_1 & S_2 are closed then the current will flow through the path -

$$V_s \rightarrow S_1 \rightarrow \text{load} \rightarrow V_o \rightarrow S_2 \rightarrow V_s.$$

so, the output voltage V_o is -

$$\boxed{V_o = V_s}$$

Again, when S_3 & S_4 are closed and S_1 & S_2 are open, current will flow through the path -

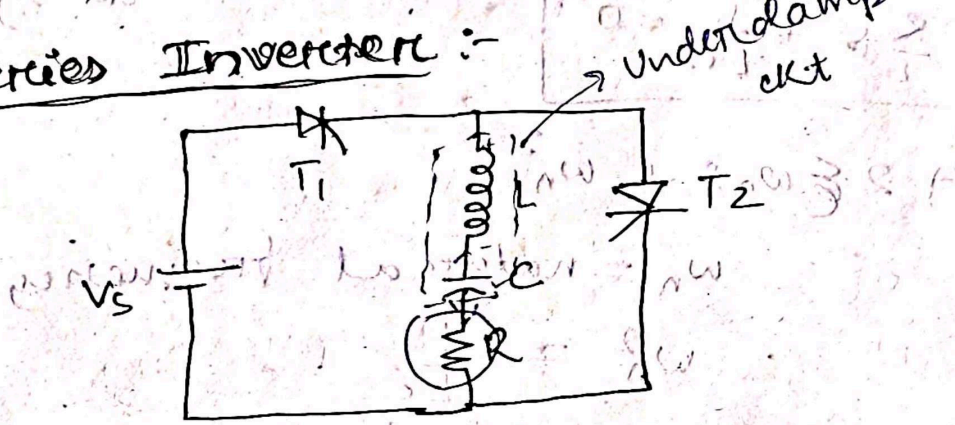
$$V_s \rightarrow S_3 \rightarrow V_o \rightarrow \text{load} \rightarrow S_4 \rightarrow V_s$$

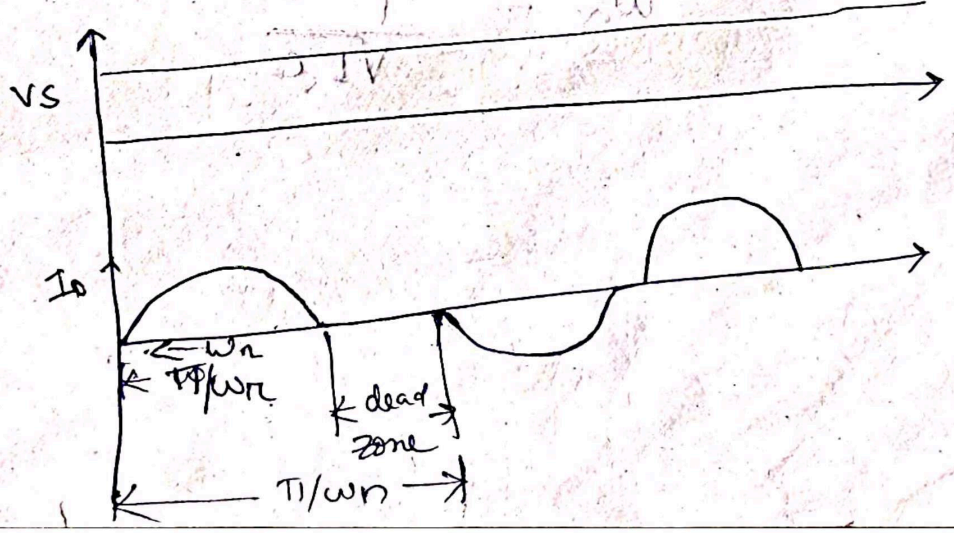
$$\boxed{V_o = -V_s}$$

* Advantages :-

→ output voltage = source voltage

* Series Inverter :-





$$V_S - V_L - V_C - V_R = 0$$

$$\Rightarrow V_S = V_L + V_C + V_R$$

$$= L\frac{di}{dt} + \frac{1}{C}\int i\,dt + iR$$

$$\Rightarrow 0 = LsI(s) + \frac{I(s)}{Cs} + I(s)R$$ [∵ Using Laplace transform]

$$\Rightarrow LsI(s) + \frac{I(s)}{Cs} + I(s)R = 0$$

$$\Rightarrow Ls + \frac{1}{Cs} + R = 0$$

$$\Rightarrow s + \frac{1}{LCs} + \frac{R}{L} = 0$$ [Dividing L on both sides].

$$\Rightarrow s^2 + \frac{1}{LC} + \frac{R}{L}s = 0$$ [Multiplying s on both sides]

$$\Rightarrow \boxed{s^2 + \frac{R}{L}s + \frac{1}{LC} = 0}$$

$$s^2 + 2\xi\omega_n s + \omega_n^2$$

ω_n = natural frequency

$$\omega_n^2 = \frac{1}{LC}$$

$$\omega_n = \frac{1}{\sqrt{LC}}.$$